STIC Search Report
EIC 2800

STIC Database Tracking Number: 124473

TO: Monica Lewis
Location: JEF5A30
Art Unit : 2822
Wednesday, June 23, 2004

Case Serial Number: 10/679431

From: Irina Speckhard
Location: EIC 2800 JEF 4B59
Phone: (571) 272-2554
irina.speckhard@uspto.gov

Search Notes

Examiner Lewis,

Please find attached prior-art search results from the patent and non-patent abstract and full-text databases. The results were based on claims and statements of technical problems and solutions. Tagged records might be worth your review as well as the rest of the references provided.

If you need further searching or have questions or comments, please let me know.

Thank you,

Irina Speckhard

Priority 2 of 7 124473

SEARCH REQUEST FORM Scientific and Technical Information Center - EIC2800

Rev. 3/15/2004 This is an experimental format -- Please give suggestions or comments to Jeff Harrison, JEF-4B68, 272-2511.

Date 6/14/04 Serial # 10/679,431 Priority Application Date ________

Your Name M. Lewis Examiner # ________

AU 2822 Phone 272-1838 Room 5A30

In what format would you like your results? Paper is the default. [✓ PAPER] DISK EMAIL

If submitting more than one search, please prioritize in order of need.

The EIC searcher normally will contact you before beginning a prior art search. If you would like to sit with a searcher for an interactive search, please notify one of the searchers.

Where have you searched so far on this case? 06-14-04 A[illegible]

Circle: USPT DWPI EPO Abs JPO Abs IBM TDB

Other: ________

What relevant art have you found so far? Please attach pertinent citations or Information Disclosure Statements. ________

What types of references would you like? Please checkmark:

Primary Refs ✓

Secondary Refs ✓

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Nonpatent Literature ___

Foreign Patents ___

Other ________

What is the topic, such as the **novelty**, motivation, utility, or other specific facets defining the desired **focus** of this search? Please include the concepts, synonyms, keywords, acronyms, registry numbers, definitions, structures, strategies, and anything else that helps to describe the topic. Please attach a copy of the abstract and pertinent claims.

Claims 15-22

Problem: See pages 1-10

Solution: " " 10-35

Staff Use Only

Searcher:

Searcher Phone: ________

Searcher Location: STIC-EIC2800, JEF-4B68

Date Searcher Picked Up: 6/23/04

Date Completed: 6/23/04

Type of Search

Structure (#) ________

Bibliographic ✓

Litigation ________

Fulltext ✓

Patent Family ✓

Vendors

STN ✓

Dialog ✓

Questel/Orbit ________

Lexis-Nexis ________

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Scientific & Technical Information Center
USPTO

STIC Search Results
Feedback Form

EIC 2800

Questions about the scope or the results of the search? Contact ***the EIC searcher or contact***:

Jeff Harrison, EIC 2800 Team Leader
571-272-2511, JEF 4B68

Voluntary Results Feedback Form

- *I am an examiner in Workgroup:* ☐ *Example: 2810*
- *Relevant prior art **found**, search results used as follows:*
  - ☐ 102 rejection
  - ☐ 103 rejection
  - ☐ Cited as being of interest.
  - ☐ Helped examiner better understand the invention.
  - ☐ Helped examiner better understand the state of the art in their technology.

Types of relevant prior art found:

- ☐ Foreign Patent(s)
- ☐ Non-Patent Literature
  (journal articles, conference proceedings, new product announcements etc.)

- *Relevant prior art **not found:***
  - ☐ Results verified the lack of relevant prior art (helped determine patentability).
  - ☐ Results were not useful in determining patentability or understanding the invention.

Comments:

Drop off or send completed forms to STIC/EIC2800, CP4-9C18

sira
Search and Information Resources Administration

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  23jun04 15:07:34 User267149 Session D1470.1

SYSTEM:OS  - DIALOG OneSearch
  File   2:INSPEC 1969-2004/Jun W2
         (c) 2004 Institution of Electrical Engineers
*File   2: Alert feature enhanced for multiple files, duplicates
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         (c) 2004 Royal Soc Chemistry
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removal, customized scheduling.  See HELP ALERT.
  File 315:ChemEng & Biotec Abs 1970-2004/May
         (c) 2004 DECHEMA
  File 350:Derwent WPIX 1963-2004/UD,UM &UP=200439
         (c) 2004  Thomson Derwent
*File 350: For more current information, include File 331 in your search.
Enter HELP NEWS 331 for details.
  File 347:JAPIO Nov 1976-2004/Feb(Updated 040607)
         (c) 2004 JPO & JAPIO
*File 347: JAPIO data problems with year 2000 records are now fixed.
Alerts have been run.  See HELP NEWS 347 for details.
  File 344:Chinese Patents Abs Aug 1985-2004/May
         (c) 2004 European Patent Office
  File 371:French Patents 1961-2002/BOPI 200209
         (c) 2002 INPI.  All rts. reserv.
*File 371: This file is not currently updating. The last update is 200209.
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Set      Items   Description
S1       41962   (NON()VOLATIL? OR NONVOLATIL?)(3N)(SEMICONDUCT? OR MEMOR?)
S2       31127   ELECTRICAL?()ERASABL?()PROGRAM?()(ROM OR MEMOR?) OR EEPROM
             OR EPROM OR ERASABL?()PROGRAM?()(MEMOR? OR ROM)
S3       20468   FLASH?(3N)MEMOR?
S4       81039   S1:S3
S5      364304   SEMICONDUCT?(3N)(SUBSTRAT? OR SURFACE? OR BASE? OR SUBSTRU-
             CT? OR UNDERSTRUCT? OR UNDERLAY? OR FOUNDATION? OR PANE? OR D-
             ISK? OR DISC? OR WAFER? OR CC=(A6855 OR A8115 OR B0520 OR B25-
             70) OR MC=(T03-A01B OR T03-A01B1) OR IC=G11B-005/704)
S6      783602    (PROTECT? OR DIELECTR? OR TUNNEL? OR STACK?)(3N)(INSULAT? -
             OR DIELECTR?)
S7      760150    (PROTECT? OR INSULAT? OR DIELECTR? OR TUNNEL? OR CAPACIT? -
             OR STACK?)(3N)(LAYER??? OR FILM??? OR COAT??? OR MULTILAYER???
              OR MULTI()LAYER????? OR SPACER??? OR INTERLAYER???? OR INTER-
             ()LAYER????? OR MULTIPLE()LAYER? ?)
S8       75968   IC=(G11C-007/00 OR H01L-021/336 OR H01L-027/115 OR H01L-02-
             9/423 OR H01L-029/76 OR H01L-029/788)
S9      144812    (CONTROL? OR FLOAT?)(3N)(GATE?? OR ELECTROD? OR INTEGRAT??-
             ??????()(CIRCUIT???????? OR LOOP? ?) OR IC OR CHIP? ?)
S10     166565   GATE??(3N)(INTEGRAT????????()(CIRCUIT???????? OR LOOP? ?) -
             OR IC OR CHIP? ? OR FLOAT? OR INSULAT? OR DIELECTR? OR ELECTR-
             OD?)
S11     286825   S9:S10
S12      32522   CAPACIT?(3N)(COUPLED OR COUPLING)
S13    1897041   CAPACIT???????? OR MC=S01-D05A3 OR IC=G01R-027/26
S14    1897041   S12:S13
S15      58318    (DRAIN OR SOURCE)(3N)REGION? ?
S16       4072   STEPPED(3N)PORTION? ?
S17    2034826   THICK?
S18     102568   SIDE()SURFAC?
S19    1349957   S6:S7
S20       5465   S4 AND S5
S21       3571   S20 AND S19
S22       2489   S21 AND S8
S23       2152   S22 AND S11
S24        314   S23 AND S14
S25         89   S24 AND S15
S26          0   S25 AND S16
S27         21   S25 AND S17
S28          0   S27 AND S18
S29         21   RD S27 (unique items)
S30         68   S25 NOT S27
S31         50   S30 AND S1
S32         14   S31 AND S2
S33         14   RD (unique items)
S34         36   S31 NOT S32
S35          1   S34 AND S3
S36         35   S34 NOT S35
S37         13   S36 AND S6
S38         13   RD (unique items)
S39         22   S36 NOT S37
S40         22   S39 AND S7
S41         22   S40 AND S11
S42         22   S41 AND S14
S43         22   RD (unique items)
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29/3,AB/1   (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX

015813169
WPI Acc No: 2003-875373/200381
XRAM Acc No: C03-247288
XRPX Acc No: N03-698928

Self-aligned multi-bit **flash memory** cell comprises **semiconductor substrate** having active region isolated, by two parallel shallow-trench-isolation regions, each filled with raised field-oxide layer, and cell region

Patent Assignee: WU C (WUCC-I)
Inventor: WU C
Number of Countries: 001 Number of Patents: 002
Patent Family:

```
Patent No      Kind   Date     Applicat No     Kind   Date      Week
US 20030193064  A1   20031016  US 2002118889    A    20020410  200381  B
US 6690058       B2  20040210  US 2002118889    A    20020410  200413
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Priority Applications (No Type Date): US 2002118889 A 20020410
Patent Details:

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Patent No  Kind Lan Pg   Main IPC    Filing Notes
US 20030193064 A1    24 H01L-029/788
US 6690058    B2       H01L-029/788
```

Abstract (Basic): US 20030193064 A1
Abstract (Basic):

NOVELTY - A self-aligned multi-bit **flash memory** cell comprises: a **semiconductor substrate** (300) of a first conductivity type having an active region isolated, by two parallel shallow-trench-isolation (STI) regions, where each of the parallel STI regions is filled with a raised field-oxide layer; and a cell region divided into a gate region formed between a common-**source region** and a common-**drain region.**

DETAILED DESCRIPTION - A self-aligned multi-bit **flash memory** cell comprises: a **semiconductor substrate** of a first conductivity type having an active region isolated, by two parallel STI regions, where each of the parallel STI regions is filled with a raised field-oxide layer; and a cell region formed on the **semiconductor substrate** and divided into three **regions**: a common-**source region**, a gate **region**, and a common-**drain region**, where the gate region is formed between the common-**source region** and the common-**drain region**.

The common-**source region** comprises a first sidewall **dielectric spacer** (307b) formed over a sidewall of the gate region, and on a portion of a first flat bed formed by a common-**source** diffusion **region** (306a), in the active region and two etched first raised field-oxide layers in the two parallel STI **regions**, a common-**source** conductive bus line formed on the first flat bed outside of the first sidewall **dielectric spacer**, and a first planarized **thick**-oxide layer (309b) formed over the common-source conductive bus line and the first sidewall **dielectric spacer**. The common-**drain region** comprises a second sidewall **dielectric spacer** (317b) formed over another sidewall of the gate region, and on a portion of a second flat bed formed by a common-**drain** diffusion **region** (316a) in the active region, and two etched second raised field-oxide layers in the two parallel STI **regions**, a common-

drain conductive bus line formed on the second flat bed outside of the second sidewall **dielectric spacer**, and a second planarized **thick**-oxide layer (319b) formed over the common-drain conductive bus line and the second sidewall **dielectric spacer**.

The gate region comprises a first **floating-gate** structure, having a first **floating-gate** layer formed on a first **gate-dielectric layer** (301c), and a second **floating-gate** structure having a second **floating-gate** layer formed on a second **gate-dielectric layer** (313b) in the active region, a spacing **dielectric layer** (312a) formed between the first **floating-gate** structure and the second **floating-gate** structure, and a planarized **control-gate** layer spaced by an intergate **dielectric layer** (320a), at least formed on the first **floating-gate** structure, the spacing **dielectric layer**, and second **floating-gate** structure. A first interconnect-metal layer (322a) together with the planarized **control-gate** is simultaneously patterned and etched, to form a word line transversely to the common-source/drain conductive bus lines.

An INDEPENDENT CLAIM is also included for a contactless multi-bit **flash memory** array, comprising: a **semiconductor substrate**; common-**source** bus-line **regions** and virtual-gate regions formed alternately and transversely to the parallel STI regions; self-aligned multi-bit **flash memory** cells formed in each of the pair of gate regions, for each of the virtual-gate regions; and word lines formed transversely to the common-source/drain conductive bus lines.

USE - For a contactless multi-bit **flash memory** array (claimed).

ADVANTAGE - The cell is scalable and its cell size can be made smaller than 4F squared. The cell has two-separated **floating-gates** for storing multi-level digital data in each **floating gate**, can be programmed by mid-channel hot-electron injection with a higher programming efficiency, and has less programming power as compared to the existing channel hot-electron injection. The contactless multi-bit **flash memory** array offers the common-source/drain conductive bus lines, as the bit lines with smaller bus-line resistances, and smaller bus-line parasitic **capacitance** with respect to the **semiconductor substrate** as compared to the buried diffusion bit lines; and offers a highly conductive metal line as a word line, with much smaller word-line resistance, and much smaller word-line parasitic **capacitance** with respect to the bit lines.

DESCRIPTION OF DRAWING(S) - The figures show cross-sectional views of a self-aligned multi-bit **flash memory** cell.

Semiconductor substrate (300)
First **gate-dielectric layer** (301c)
Common-**source** diffusion **region** (306a)
First sidewall **dielectric spacer** (307b)
First planarized **thick**-oxide layer (309b)
Spacing **dielectric layer** (312a)
Second **gate-dielectric layer** (313b)
Common-**drain** diffusion **region** (316a)
Second sidewall **dielectric spacer** (317b)
Second planarized **thick**-oxide layer (319b)
Intergate **dielectric layer** (320a)
First interconnect-metal layer (322a)
Masking **dielectric layer** (323a)

pp; 24 DwgNo 2A/6

29/3,AB/2 (Item 2 from file: 350)
DIALOG(R)File 350:Derwent WPIX

015658478
WPI Acc No: 2003-720663/200368
XRAM Acc No: C03-198270
XRPX Acc No: N03-576139
Scalable dual-bit **flash memory** array comprises, gate regions and common bus-line regions formed alternately over **semiconductor substrate** and transversely to parallel shallow-trench-isolation regions
Patent Assignee: WU C (WUCC-I)
Inventor: WU C
Number of Countries: 001 Number of Patents: 002
Patent Family:

```
Patent No      Kind   Date     Applicat No    Kind   Date      Week
US 20030141541  A1   20030731  US 200258427    A   20020130  200368  B
US 6627927      B2   20030930  US 200258427    A   20020130  200372
```

Priority Applications (No Type Date): US 200258427 A 20020130
Patent Details:

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Patent No  Kind Lan Pg   Main IPC    Filing Notes
US 20030141541 A1    26 H01L-029/76
US 6627927     B2       H01L-029/76
```

Abstract (Basic): US 20030141541 A1
Abstract (Basic):

NOVELTY - A scalable dual-bit **flash memory** array comprises gate regions and common bus-line regions formed alternately over a **semiconductor substrate** (100) and transversely to parallel shallow-trench-isolation (STI) regions, where the gate regions are formed by a masking photoresist step and are scalable. Each of the common bus-line regions comprises common conductive bus-line (119b) formed over a first flat bed.

DETAILED DESCRIPTION - A scalable dual-bit **flash memory** array comprises:

(a) a **semiconductor substrate** of a first conductivity type;

(b) parallel STI regions and active regions formed alternately on the **semiconductor substrate**, where each of the parallel STI regions is filled with a raised field-oxide layer;

(c) gate regions and common bus-line regions formed alternately over the **semiconductor substrate** and transversely to the parallel STI regions, where the gate regions are formed by a masking photoresist step and are scalable;

(d) common-**source** diffusion **regions** of a second conductivity type formed in the **semiconductor substrate** of the active regions along the common bus-line regions;

(e) a first flat bed formed between a pair of **dielectric-spacer** structures in each of the common bus-line regions and alternately formed by the common-**source** diffusion **region** and a first etched raised field-oxide layer, where each of the **dielectric-spacer** structures is formed over each sidewall of the gate region, and each of the common bus-line regions comprises from top to bottom a planarized **thick**-oxide layer (121a) formed over the pair of **dielectric-spacer** structures, a silicide layer (120b), and a common conductive bus-line formed over the first flat bed;

(f) a stack-gate transistor region formed in each side portion of the gate region and a selector region formed between the stack-gate transistor regions, where the stack-gate transistor region comprises from top to bottom a sidewall **dielectric spacer** (118b, 122a) formed over a nearby sidewall of the common bus-line region, an elongated **control-gate** layer (108b) formed over an intergate **dielectric layer** (107b), and integrated **floating-gate** layers, and the selector region comprises planarized conductive islands (126b) formed over a second flat bed above the active regions; and

(g) select lines formed alternately above the active regions and transversely to the parallel STI regions, and electrically connected to the planarized conductive islands along the active regions, where each of the select lines is formed by a metal layer together with the planarized conductive islands simultaneously patterned and etched by a hard masking layer.

USE - Used as scalable dual-bit **flash memory** array, e.g. NOR-(sic) type **flash memory** array, for high-density mass storage applications.

ADVANTAGE - The dual-bit **flash memory** cells offer a cell size/bit smaller than 4-minimum-feature-size (F2). It offers a high-speed erasing anode for erasing the stored electrons in the integrated **floating-gate** layer, to a common-source conductive bus line. It offers a larger coupling ratio for a **floating-gate** layer using a self-aligned integrated **floating-gate** layer, without enlarging the isolation area. The memory array offers a shallow-trench-isolation structure for the dual-bit **flash memory** cells in different columns or rows. It offers a common-source conductive bus line with smaller bus-line resistance and **capacitance**, as compared to those of a buried diffusion line. It offers a better density speed power product as compared to a NAND-(sic) type array.

DESCRIPTION OF DRAWING(S) - The figure shows a cross-sectional view of a dual-bit **flash memory** cell.

Semiconductor substrate (100)
Intergate **dielectric layer** (107b)
Elongated **control-gate** layer (108b)
Lightly-doped diffusion region (112a)
Thin **tunneling** poly-oxide **layer** (114a)
Conductive erasing anode (116d)
Sidewall **dielectric spacer** (118b, 122a)
Common conductive bus-line (119b)
Silicide layer (120b)
Planarized **thick**-oxide layer (121a)
Implanted region (123)
Heavily-doped diffusion region (124a)
Gate-dielectric layer (125)
Planarized conductive islands (126b)
Metal layer (127a)
Masking **dielectric layer** (128a)
pp; 26 DwgNo 2Aa/5

29/3,AB/3 (Item 3 from file: 350)
DIALOG(R)File 350:Derwent WPIX

015504579

WPI Acc No: 2003-566726/200353
XRAM Acc No: C03-152841
XRPX Acc No: N03-450523

Scalable stack-gate **flash memory** cell for high density memory system has substrate, cell **region,** common **source** and **drain** diffusion **regions,** flat beds, common **source** and drain conductive **layers,** and scalable **stack**-gate structure

Patent Assignee: WU C (WUCC-I)
Inventor: WU C
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 6570214	B1	20030527	US 200285016	A	20020301	200353	B

Priority Applications (No Type Date): US 200285016 A 20020301
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 6570214	B1		23	H01L-029/788	

Abstract (Basic): US 6570214 B1
Abstract (Basic):

NOVELTY - Scalable stack-gate **flash memory** cell comprises **semiconductor substrate** of first conductivity type, cell region with active region and two shallow-trench-isolation (STI) **regions,** common **source** diffusion **region** of second conductivity type, two flat beds, common source conductive layer, common **drain** diffusion **region,** common **drain** conductive **layer,** and scalable **stack**-gate structure.

DETAILED DESCRIPTION - A scalable stack-gate **flash memory** cell comprises: a **semiconductor substrate** (300) of the first conductivity type, a cell region with an active region and two shallow-trench-isolation (STI) **regions,** a common **source** diffusion **region** of a second conductivity type, first and second flat beds, a common source conductive layer, a common **drain** diffusion **region,** a common **drain** conductive **layer,** and a scalable **stack**-gate structure.

The STI is formed on the **semiconductor substrate** and is divided into common source, gate, and common **drain regions.** The gate **region** is between the common **source** and common **drain regions** with its **control-gate** length. The **control-gate** length is defined by a sidewall **dielectric spacer** (321a) formed over a sidewall of the common **source region.** The STIR is filled with a raised field oxide layer (308b).

The common **source** diffusion **region** is formed in the **semiconductor substrate** by implanting doping impurities in a self-aligned manner into the active **region** in the common **source region.**

The first flat bed is formed by common **source** diffusion **region** and nearby first etched raised field-oxide layers.

The first sidewall **dielectric spacer** is formed over the sidewall of the gate region and on the portion of the first flat bed.

The common source conductive layer is formed over the first flat bed outside of the first sidewall **dielectric spacer** (309b). A first planarized **thick**-oxide layer (312b) is formed over the common source conductive layer and the first sidewall **dielectric spacer.**

The common **drain** diffusion **region** is formed in the **semiconductor substrate** by implanting doping impurities in a self-aligned manner into the active **region** in the common

drain region.

The second flat bed is formed by the common **drain** diffusion **region** and the second etched raised field-oxide layers.

A second side wall **dielectric spacer** is formed over another sidewall of the gate region and on a portion of the second flat bed.

The common drain conductive layer is formed over the second flat bed outside the second sidewall **dielectric spacer**.

A second planarized **thick**-oxide layer is formed over the common drain conductive layer and the second sidewall **dielectric spacer**.

The scalable stacked gate structure is formed in the gate region.

The top through the bottom of stack-gate structure comprises a planarized **control-gate** (306c), an intergate **dielectric layer** (350b), a **floating gate** layer (302a), and a thin **tunneling-dielectric layer** (301a, 301c) formed on the **semiconductor substrate**.

USE - Useful in high density memory system.

ADVANTAGE - The invention eliminates the increase buried bit line junction **capacitance**, as well as the decrease in cell width. It has a gate length that is easily scaled down without increasing the bit-line resistance and decreases the read/erasing speed. It has higher parasitic **capacitance** between the word lines and the common buried diffusion bit lines is reduced.

DESCRIPTION OF DRAWING(S) - The figure shows a process steps and the cross-sectional view of the formation of the contactless scalable stack-gate **flash memory** array.

Semiconductor substrate (300)
Thin **tunneling-dielectric layer** (301a, 301c)
Floating gate layer (302a)
Raised field oxide layer (304b)
Planarized **control-gate** (306c)
Lightly doped diffusion region (308a)
Heavily-doped diffusion region(309b) Sidewall **dielectric spacers** (308b)
Metal-silicide layer (311b)
Thick-oxide layer (312b)
Implanted region (314b)
Double-diffused drain structure (315a)
Word line (321a)
Masking **dielectric layer** (322a)
Integrate **dielectric layer** (350b)
pp; 23 DwgNo 4N/4

29/3,AB/4 (Item 4 from file: 350)
DIALOG(R)File 350:Derwent WPIX

014459348
WPI Acc No: 2002-280051/200232
XRAM Acc No: C02-082311
XRPX Acc No: N02-218702

Nonvolatile memory cell, e.g. **non volatile** random access **memory**, has vertical electrical via which couples plate of **capacitor** through **insulator layer** to **gate** of transistor

Patent Assignee: CLOUD E H (CLOU-I); NOBLE W P (NOBL-I); MICRON TECHNOLOGY INC (MICR-N)
Inventor: CLOUD E H; NOBLE W P

Number of Countries: 001 Number of Patents: 002

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 20020024083	A1	20020228	US 99259493	A	19990226	200232	B
US 6380581	B1	20020430	US 99259493	A	19990226	200235	

Priority Applications (No Type Date): US 99259493 A 19990226

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 20020024083	A1		20	G11C-011/34	
US 6380581	B1			H01L-021/70	

Abstract (Basic): US 20020024083 A1

Abstract (Basic):

NOVELTY - **Nonvolatile memory** cell (200A-B) comprises transistor (210A-B), a **capacitor** (220A-B), and a vertical electrical via (230A-B). The via couples a first plate (223) of the **capacitor** through an **insulator layer** (232) to **gate** (212A-B) of the transistor.

DETAILED DESCRIPTION - INDEPENDENT CLAIMS are also included for:

(I) a **non volatile memory** array (200) comprising the above-mentioned **non volatile memory** cells, a wordline coupled to the top plate of the stacked **capacitor**, a bit line (219A-B) coupled to a **drain region** (216A-B) of metal oxide semiconductor field effect transistor (MOSFET), and a sourceline (217A-B) coupled to a **source region** (215A-B) of the MOSFET;

(II) an electronic system comprising a processor, a dynamic random access memory (DRAM) chip, and a system bus coupling the processor to the DRAM chip;

(III) a method for forming a **non volatile memory** cell on a DRAM chip comprising forming a MOSFET in a substrate on the DRAM chip, forming a stacked **capacitor** above the gate of the MOSFET using a DRAM process, and forming an electrical contact using a DRAM process;

(IV) a method of operating a memory cell comprising controlling a charge on the gate of MOSFET and on the bottom plate of the **capacitor** to regulate a threshold voltage for the memory cell; and

(V) a method of programming a memory device comprising grounding a **source region** for MOSFET, applying a **control gate** voltage to the top plate, and applying a drain voltage of approximately half of the **control gate** voltage to a **drain region** of the MOSFET.

USE - Used as **non volatile** access **memory**, e.g. electrically erasable and programmable read only **memory**, or a **flash memory** cell (claimed).

ADVANTAGE - Operates with lower programming voltages than that used by conventional **non volatile memory** cells, yet still hold sufficient charge to withstand the effects of parasitic **capacitances** and noise due to circuit operation, thus realizing the requirements of low power density packed integrated circuits for smaller, portable devices.

DESCRIPTION OF DRAWING(S) - The drawing shows a perspective view of a **non volatile memory** array.

memory array (200)
nonvolatile memory cell (200A-200B)
transistor (210A-210B)
gate (212A-212B)
source region (215A-215B)
drain region (216A-216B)

```
        sourceline (217A-217B)
        bit line (219A-219B)
        capacitor (220A-220B)
        plate (223)
        electrical via (230A-230B)
        insulator layer (232)
        pp; 20 DwgNo 2/8


 29/3,AB/5     (Item 5 from file: 350)
DIALOG(R)File 350:Derwent WPIX
(c) 2004  Thomson Derwent. All rts. reserv.

013430209
WPI Acc No: 2000-602152/200057
XRAM Acc No: C00-180265
XRPX Acc No: N00-445519
  Method of manufacturing semiconductor device e.g., floating
  gate field effect transistor involves forming a floating
  gate dielectric, floating gate, interlayer
  dielectric and control gate on an active region of a
  semiconductor body
Patent Assignee: KONINK PHILIPS ELECTRONICS NV (PHIG  ); US PHILIPS CORP
  (PHIG  )
Inventor: MONTREE A H; SCHMITZ J; WOERLEE P H
Number of Countries: 023  Number of Patents: 006
Patent Family:
Patent No      Kind   Date     Applicat No     Kind   Date     Week
WO 200055896    A1  20000921  WO 2000EP1521    A   20000224  200057  B
EP 1082760      A1  20010314  EP 2000916865    A   20000224  200116
                              WO 2000EP1521    A   20000224
KR 2001025029   A   20010326  KR 2000712846    A   20001116  200161
US 6368915      B1  20020409  US 2000527203    A   20000316  200227
JP 2002539637   W   20021119  JP 2000606041    A   20000224  200281
                              WO 2000EP1521    A   20000224
TW 498557       A   20020811  TW 2000103817    A   20000303  200331

Priority Applications (No Type Date): EP 99200815 A 19990317
Patent Details:
Patent No  Kind Lan Pg   Main IPC    Filing Notes
WO 200055896  A1 E  28 H01L-021/336
   Designated States (National): JP KR
   Designated States (Regional): AT BE CH CY DE DK ES FI FR GB GR IE IT LU
   MC NL PT SE
EP 1082760    A1 E     H01L-021/336  Based on patent WO 200055896
   Designated States (Regional): AT BE CH CY DE DK ES FI FR GB GR IE IT LI
   LU MC NL PT SE
KR 2001025029 A        H01L-021/336
US 6368915    B1       H01L-021/336
JP 2002539637 W     30 H01L-021/8247 Based on patent WO 200055896
TW 498557     A        H01L-029/788

Abstract (Basic): WO 200055896 A1
Abstract (Basic):
        NOVELTY - Semiconductor device manufacture involves applying a
    first insulating layer in a recess in a dielectric
    layer to form a floating gate dielectric,
    filling the recess with a first conductive layer which is shaped to
    form a floating gate, covering floating gate with a
    second insulating layer forming an inter-gate
```

dielectric and forming a second conductive layer which is shaped to form a **control gate.**

DETAILED DESCRIPTION - A semiconductor device comprises a semiconductor body (1) which is provided at a surface with a **non-volatile memory** element having a **floating gate** (21) situated between an overlapping **control gate** (27) and a channel region (13) which is situated in the semiconductor body and extends between the **source** and **drain regions.** Semiconductor device manufacture involves defining an active region (4) of a first conductivity at the **surface** (2) of a **semiconductor** body (1). A **floating gate dielectric** (19) is provided to which a **floating gate** (21) is applied. The **floating gate** has a flat surface portion (22) extending parallel to the **surface** of the **semiconductor** body and has sidewall portions (23) extending perpendicularly to the **surface** of the **semiconductor** body. The **floating gate** (21) is provided with an inter-**gate dielectric** (25) to which the **control gate** (27) is applied. The **control gate** is **capacitatively coupled** with the flat surface portion of the **floating gate** and with at least the sidewall portions of the **floating gate** situated adjacent to the source (11) and drain zones (12). After defining the active region, a patterned layer is applied which acts as a mask during the formation of source and drain zones of a second conductivity type in the semiconductor body. A **dielectric layer** (14) of sufficient **thickness** to cover the patterned layer is formed. Part of the **dielectric layer** is removed by a material removing treatment, until the patterned layer is exposed. The patterned layer is removed forming a recess in the **dielectric layer.** A first **insulating layer** is formed in the recess to form the **floating gate dielectric** (19) of the memory element. A first conductive layer which fills the recess is applied to the first **insulating layer.** The first conductive layer is shaped into the **floating gate** (21) by means of masked etching. The **floating gate** is covered by a second **insulating layer** providing an inter-**gate dielectric** (25) of the memory element. A second conductive layer is applied to the second **insulator layer.** The second conductive layer is shaped into the overlapping **control gate** (27).

USE - The method is used in manufacturing a **floating gate** field effect transistor. The method maybe used in the manufacture of complementary metal oxide semiconductor (CMOS) and BiCMOS integrated circuits.

ADVANTAGE - Induction of parasitic **capacitances** between the overlapping **control gate** and the semiconductor body is suppressed. Hence an increase in supply voltage is counteracted.

DESCRIPTION OF DRAWING(S) - The diagram shows a cross-sectional view of the semiconductor device.

Semiconductor body (1)
Surface (2)
Thick oxide field insulating regions (3)
Active region (4)
Source zone (11)
Drain zone (12)
Channel region (13)
Dielectric layer (14)
Impurity region (16)
Floating gate dielectric (19)
Floating gate (21)

Flat surface portion (22)
Sidewall portions (23)
Inter-**gate dielectric** (25)
Control gate (27)
pp; 28 DwgNo 12/14

29/3,AB/6 (Item 6 from file: 350)
DIALOG(R)File 350:Derwent WPIX

013177536
WPI Acc No: 2000-349409/200030
XRAM Acc No: C00-106144
XRPX Acc No: N00-261763

Forming **source region** in semiconductor device, involves forming of field oxide **regions** after self-aligning **source region** to stacked gate structures

Patent Assignee: TAIWAN SEMICONDUCTOR MFG CO (TASE-N)
Inventor: HSU C; LIANG M; LIN R
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 6054348	A	20000425	US 9879880	A	19980515	200030	B

Priority Applications (No Type Date): US 9879880 A 19980515
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 6054348	A		9	H01L-021/336	

Abstract (Basic): US 6054348 A
Abstract (Basic):

NOVELTY - A **source region** is formed by:

(a) forming stacked gate structures on the substrate (1);

(b) forming a **source region** in a first region which is self-aligned to the stacked gate structures; and

(c) forming field oxide (FOX) regions (12) in a second region between rows of stacked gate structure normal in direction to the first region

DETAILED DESCRIPTION - An INDEPENDENT CLAIM is also included for a method of fabricating an electrical programmable read only memory (**EPROM**) device. The method includes:

(i) forming a **gate insulator layer**;

(ii) depositing a first polysilicon layer;

(iii) forming an oxidized silicon nitride on oxide (ONO) layer;

(iv) patterning to form stacked gate structures;

(v) forming a photoresist shape;

(vi) forming a **source region** in the first region;

(vii) depositing a composite **insulator layer** with silicon nitride, overlying a silicon oxide layer;

(viii) patterning a composite **insulator layer** on an exposed second region;

(ix) forming a FOX;

(x) removing remaining composite **insulator layer**; and

(xi) forming a self aligned **drain region** in a third region.

USE - For forming a **source region** in a semiconductor memory device, e.g., an **EPROM**.

ADVANTAGE - Places FOX regions in desired locations, eliminating the need for removal of unwanted FOX regions. It eliminates the possible damage in the substrate during the FOX removal procedure. It results in bird's beak formation under the stacked gate structures. It decreases a **capacitance** component, which enables an increase in the coupling ratio of the device.

DESCRIPTION OF DRAWING(S) - The figure shows a schematic top view of a **source region.**

Semiconductor substrate (1)
Gate insulator layer (2)
First polysilicon layer (3)
ONO layer (4)
Polysilicon layers (5)
Stacked gate structures (6)
Source region (8)
FOX regions (12)
pp; 9 DwgNo 4b/4

29/3,AB/7 (Item 7 from file: 350)
DIALOG(R)File 350:Derwent WPIX

010663609
WPI Acc No: 1996-160563/199616
XRPX Acc No: N96-134480

Integrated circuit chip mfr. method with **EEPROM** - by depositing mask defining **source-drain regions** of select and memory transistors, mask defining tunnel region of memory transistor and mask defining **floating gate** and **gate** of each select transistor

Patent Assignee: NAT SEMICONDUCTOR CORP (NASC)
Inventor: CACHARELIS P J; NARAHARI N; PERRY J R
Number of Countries: 018 Number of Patents: 008
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
WO 9607203	A1	19960307	WO 95US11037	A	19950829	199616	B
EP 725980	A1	19960814	EP 95931647	A	19950829	199637	
			WO 95US11037	A	19950829		
US 5550072	A	19960827	US 94298239	A	19940830	199640	
			US 94325855	A	19941019		
US 5591658	A	19970107	US 94298239	A	19940830	199708	
			US 95469575	A	19950606		
US 5894147	A	19990413	US 94298239	A	19940830	199922	
			US 95482319	A	19950606		
EP 725980	B1	20011205	EP 95931647	A	19950829	200203	
			WO 95US11037	A	19950829		
DE 69524376	E	20020117	DE 624376	A	19950829	200213	
			EP 95931647	A	19950829		
			WO 95US11037	A	19950829		
KR 355840	B	20030106	WO 95US11037	A	19950829	200337	
			KR 96701955	A	19960416		

Priority Applications (No Type Date): US 94298239 A 19940830; US 94325855 A 19941019; US 95469575 A 19950606; US 95482319 A 19950606

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
WO 9607203	A1	E	38	H01L-021/8247	

Designated States (National): DE KR
Designated States (Regional): AT BE CH DE DK ES FR GB GR IE IT LU MC NL PT SE

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 725980	A1	E	38	H01L-021/8247	Based on patent WO 9607203

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   Designated States (Regional): DE FR GB
US 5550072     A     28 H01L-021/8247 Div ex application US 94298239
US 5591658     A     27 H01L-021/8247 Div ex application US 94298239
US 5894147     A        H01L-029/788  Cont of application US 94298239
EP 725980      B1 E     H01L-021/8247 Based on patent WO 9607203
   Designated States (Regional): DE FR GB
DE 69524376    E        H01L-021/8247 Based on patent EP 725980
                                      Based on patent WO 9607203
KR 355840      B        H01L-021/8247 Previous Publ. patent KR 96705356
                                      Based on patent WO 9607203
```

Abstract (Basic): WO 9607203 A

The method uses three masking steps in addition to those required for the basic CMOS transistors in the chip. A first mask layer defines **source-drain regions** of select and memory transistors within an **EEPROM** cell. A second mask **layer** defines a **tunnelling** region of the memory transistor and a third mask layer defines a **floating gate** of the memory transistor and a gate of the select transistor.

A **control gate** of the memory transistor is formed using the same mask used to define the gates of the CMOS transistors. The third and fourth mask layers may also be used to form the lower and upper electrodes respectively of a **capacitor.**

USE/ADVANTAGE - For smart analogue chips used in antilock braking systems. Has reduced number of processing steps.

Dwg.20A/46

Abstract (Equivalent): US 5591658 A

A process of fabricating a memory transistor, said process comprising the steps of:

providing a **semiconductor substrate:**

forming a pair of **source/drain regions** at a surface of said substrate, said **source/drain regions** being separated by a channel region;

forming a gate oxide layer over said **source/drain regions** and said channel region;

etching said gate oxide layer to expose a portion of said surface of said substrate, said portion comprising a tunnel oxide region, said tunnel oxide region overlying one of said **source/drain regions;**

growing a **tunnel** oxide **layer** in said **tunnel** oxide region;

depositing a first conductive layer over said gate oxide **layer** and said **tunnel** oxide **layer;**

depositing an **insulating layer** over said first conductive layer;

forming a first mask over said **insulating layer;**

etching said **insulating layer** in areas thereof not covered by said first mask;

etching said first conductive layer to form a **floating gate**, said **floating gate** covering said tunnel oxide region and having a peripheral edge which surrounds said tunnel oxide region;

depositing a second conductive **layer** over said **insulating layer;**

forming a second mask over said second conductive layer; and

etching said second conductive layer in areas thereof not covered by said second mask to form a **control gate,** said **control gate** being sized and positioned such that a peripheral region of said **floating gate** extends laterally outward beyond said **control gate** along an entire length of

said peripheral edge of said **control gate.**
Dwg.20a/21
US 5550072 A
A method of fabricating an IC device including an **EEPROM** cell, said method comprising performing the following steps in the order indicated:
providing a semiconductor member having a flat surface;
forming a first mask layer over said semiconductor member to define **source/drain regions** of a select transistor and a memory transistor within said **EEPROM** cell;
implanting dopant into said semiconductor member using said first mask layer to form said **source/drain regions;**
removing said first mask layer;
growing a **thick** oxide on said **surface** of said **semiconductor** member;
forming a second mask layer over said **thick** oxide **layer** to define a **tunnel** region of said memory transistor;
etching said **thick** oxide layer using said second mask layer;
removing said second mask layer;
depositing a first conductive **layer** and depositing a **dielectric layer** over said first conductive layer;
forming a third mask layer over said first conductive **layer** and said **dielectric layer** to define a **floating gate** of said memory transistor and a gate of said select transistor;
etching said first conductive **layer** and said **dielectric layer** using said third mask layer to form the **floating gate** of said memory transistor and the gate of said select transistor;
removing said third mask layer;
growing a thin oxide layer on said **surface** of said **semiconductor** member in a region where a first low-voltage MOSFET is to be formed;
depositing a second conductive **layer** over said **dielectric layer** and said thin oxide layer;
forming a fourth mask layer to define a **control gate** of said memory transistor and a gate of said first low-voltage MOSFET; and

etching said second conductive layer through said fourth mask layer to form the **control gate** of said memory transistor and the gate of said first low-voltage MOSFET.
Dwg.20a/21

29/3,AB/8 (Item 8 from file: 350)
DIALOG(R)File 350:Derwent WPIX

010381896
WPI Acc No: 1995-283210/199537
Related WPI Acc No: 1996-077160
XRAM Acc No: C95-127834
Electrically programmable read only memory device - having a dual sidewall **floating gate** structure
Patent Assignee: TAIWAN SEMICONDUCTOR MFG CO LTD (TASE-N)
Inventor: SUNG-MU H
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 5440158	A	19950808	US 94270737	A	19940705	199537	B

```
Priority Applications (No Type Date): US 94270737 A 19940705
Patent Details:
Patent No  Kind Lan Pg   Main IPC    Filing Notes
US 5440158    A     10 H01L-029/76
```

Abstract (Basic): US 5440158 A

Fabricating an improved **EPROM** device having dual sidewall **float gates** comprises: forming a thin **insulating layer** on a surface of a monocrystalline Si **semiconductor substrate** having a background impurity of a first conductivity type; depositing a layer of oxidn. resistant material over the thin **insulating layer**; patterning the oxidn. resistant masking layer to form openings that define field oxide areas on the substrate; forming **thick** field oxide regions in the exposed areas in the substrate adjacent to the surface; depositing, exposing, and developing a resist layer on the substrate surface to cover at least a central area between the field oxide regions; removing the portions of the oxidn. resistant masking layer not covered by the resist layer forming an oxidn. resistant masking line with vertical sidewalls; removing the resist layer; implanting first conductivity type impurity ions into the substrate using the masking line and the field oxide as masks forming first doped regions for threshold voltage adjustment; removing the exposed thin **insulating layer;** forming a **tunnel** oxide **layer** on the substrate surface; depositing a first conformal polycrystalline Si layer over the substrate; anisotropically etching the first conformal polycrystalline Si layer forming dual **floating gates** on the vertical sidewalls of the oxidn. resistant masking line; obliquely ion implanting impurity ions of a first conductivity type into the substrate utilising the dual **floating gates**, field oxide regions and masking line as masks forming second doped regions in the substrate located on either side of the **floating gate** structures; removing the oxidn. resistant masking line leaving the dual spaced **floating gates**; ion implanting second conductivity type impurity ions into the substrate utilizing the dual **floating gates** as masks to form a central **source region** located between the **floating gate** structures and 2 spaced **drain regions** in the substrate located on either side of the **floating gate** structures; **thickening** the tunnel oxide **layer** forming a **thick insulation layer**; forming a composite layer over the surface of the substrate; depositing a second polycrystalline Si layer over the composite layer; forming a polycide layer on top of the second polycrystalline Si layer; etching the polycide layer, the second polycrystalline Si layer, the composite layer and the **floating gates** to form word lines in the second polycrystalline Si and polycide layers; forming electrical contacts and metallurgy lines with appropriate passivation, and connecting the source, drain and gate elements to form an **EPROM** device.

USE - Producing EPROMs and flash **EPROM** devices.

ADVANTAGE - Improved structure having dual sidewall **floating gate** structure; reduces cell size; increased **capacitive coupling** between **floating gate** and **control gate**; reduced mfg. costs.

(Dwg.9/11

29/3,AB/9   (Item 9 from file: 350)
DIALOG(R)File 350:Derwent WPIX

010331924
WPI Acc No: 1995-233616/199531
XRPX Acc No: N95-182107

Double polysilicon level for **non volatile memory** - has channel between **source** and **drain regions** that includes area extending into lateral zones beneath gates and perpendicular to source drain direction

Patent Assignee: SGS THOMSON MICROELTRN SRL (SGSA); SGS THOMSON MICROELTRN SARL (SGSA)
Inventor: KRAMER A; SABATINI M
Number of Countries: 006 Number of Patents: 005

```
Patent Family:
Patent No     Kind   Date      Applicat No     Kind   Date      Week
EP 661756      A1   19950705   EP 93830538      A    19931231  199531  B
JP 7326680     A    19951212   JP 94325655      A    19941227  199607
US 5592418     A    19970107   US 95367068      A    19950103  199708
EP 661756      B1   19971029   EP 93830538      A    19931231  199748
DE 69314964    E    19971204   DE 614964        A    19931231  199803
                               EP 93830538      A    19931231

Priority Applications (No Type Date): EP 93830538 A 19931231
Patent Details:
Patent No   Kind Lan Pg   Main IPC    Filing Notes
EP 661756     A1 E    8 H01L-029/788
   Designated States (Regional): DE FR GB IT
JP 7326680    A       5 H01L-021/8247
US 5592418    A      14 G11C-011/40
EP 661756     B1 E    9 H01L-029/788
   Designated States (Regional): DE FR GB IT
DE 69314964   E         H01L-029/788  Based on patent EP 661756
```

Abstract (Basic): EP 661756 A

The **non-volatile memory** cell includes a double level of polycrystalline silicon. The **FLASH EEPROM memory** cell (30) has a **source region** (38) and a **drain region** (31) with contacts (35, 39) defined in the **substrate** of the **semiconductor** material. The channel region (34) extends between the **source** and **drain regions**.

The channel also extends in two lateral zones adjacent to the main zone beneath the **floating gate** (33) and the **control gate** (32). The channel region is defined in the substrate by **thick** oxide regions. The normal programming of the cell is not affected by these changes.

ADVANTAGE - Provides an analog computing device with high density and small integration area.

Dwg.7/8

Abstract (Equivalent): EP 661756 B

Non-volatile memory cell with double level of polycrystalline silicon integrated monolithically in a **substrate** of **semiconductor** material and comprising a **source region** (38), a **drain region** (31), a channel **region** (34) between said **source** and **drain regions**, a **floating gate** (33), and a **control gate** (32) defined in said levels of polycrystalline silicon and separated by at least one **layer of dielectric** material (37) and both extending at least on the channel region which is covered by a thin **layer of dielectric** material (36) and characterised in that the width of the channel region is in at least one part greater than any of the parts of the channel **region** adjoining the **source** and **drain regions.**

Dwg.1/8

Abstract (Equivalent): US 5592418 A

An integrated circuit analog memory, comprising:

a memory cell comprising

source and drain diffusions of a first type, and a channel **region** separating said **source** diffusion from said drain diffusion;

a first conductive thin film gate **layer,** overlying and **capacitively coupled** to and insulated from said channel region; and

a second conductive thin film gate **layer,** overlying and **capacitively coupled** to and insulated from said first conductive thin film gate layer and said channel region;

wherein each of said gate layers has a width over said channel which is greater than the width of said channel near said **source** and **drain regions;**

sensing circuitry, connected to sense, and to provide a voltage output corresponding to, the charge stored in said memory cell, without applying current between source and drain thereof; and

write circuitry, connected to controllably inject charge into said first conductive thin film layer of said memory cell;

wherein said channel includes a widened portion, beneath said **floating gate** which is wider than portions of said channel nearer said **source** and **drain regions.**

Dwg.11/21

29/3,AB/10 (Item 10 from file: 350)
DIALOG(R)File 350:Derwent WPIX

010127128
WPI Acc No: 1995-028379/199504
XRAM Acc No: C95-060759
XRPX Acc No: N95-103458

Non-volatile semiconductor memory device - having offset region immediately under side wall gate functioning as inversion layer

Patent Assignee: ROHM CO LTD (ROHL)
Inventor: NAKAO H; OZAWA T; SHIMOJI N; TSURUTA M
Number of Countries: 002 Number of Patents: 003
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
JP 6314795	A	19941108	JP 93104512	A	19930430	199504	B
US 5402374	A	19950328	US 94235326	A	19940429	199518	
JP 3317459	B2	20020826	JP 93104512	A	19930430	200263	

Priority Applications (No Type Date): JP 93104512 A 19930430
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
JP 6314795	A		15	H01L-029/788	
US 5402374	A		21	G11C-011/34	
JP 3317459	B2		13	H01L-021/8247	Previous Publ. patent JP 6314795

Abstract (Basic): US 5402374 A

Non-volatile memory device comprises: (a) a **semiconductor substrate** of a predetermined conductivity type; (b) a **source region** and a **drain region** of a second conductivity type opposite to the first conductivity type, which are formed spaced apart from each other by a predetermined distance on a surface layer of the substrate; (c) a **tunnel insulation film** interposed between the **source region** and the **drain region** having such a **thickness** that charges produced in a channel region so formed as to be able to pass therethrough by tunnelling, which is formed spaced apart from the **source region** by a predetermined offset distance on the channel region; (d) a **floating gate** formed on the **tunnel insulation film** for storing the charges which passed through the **tunnel insulation** film by **tunnelling**; (e) **capacitor insulation film** formed on the **floating gate** for trapping the charges stored in the **floating gate** so as not to escape; (f) a **control gate** formed on the **capacitor insulation film**, to which a predetermined control voltage is applied; (g) a sidewall gate formed above the remaining channel region on the side of the **source region** where the **tunnel insulation film** is not formed; (h) insulating means for **insulating** the side wall **gate** from the channel region, the **floating gate**, the **capacitor insulation film** and the **control gate**. A **non-volatile memory** circuit is also claimed.

ADVANTAGE - Increased number of times of rewritability; instantaneously rewriting information preventing a write disturbance (a drain disturbance and/or a gate disturbance) at the time of writing information.

Dwg.1/12

29/3,AB/11 (Item 11 from file: 350)
DIALOG(R)File 350:Derwent WPIX

009842506
WPI Acc No: 1994-122362/199415
XRPX Acc No: N98-422880

Semiconductor memory device for storing information as electric charges - has **tunnelling** oxide **layer** on surface of polycrystalline layer, with **floating gate electrode** on tunnelling layer and intervening insulating **layer** on **floating gate**, under **control gate**

Patent Assignee: FUJITSU LTD (FUIT)
Inventor: ITO T
Number of Countries: 002 Number of Patents: 002
Patent Family:

```
Patent No     Kind   Date     Applicat No    Kind   Date     Week
JP 6069515     A   19940311  JP 92220122     A   19920819  199415  B
US 5818083     A   19981006  US 93108494     A   19930818  199847
                             US 95521461     A   19950830
                             US 97825057     A   19970327
```

Priority Applications (No Type Date): JP 92220122 A 19920819
Patent Details:

```
Patent No  Kind Lan Pg   Main IPC     Filing Notes
JP 6069515    A      5 H01L-029/788
US 5818083    A     15 H01L-029/788  Cont of application US 93108494
                                     Cont of application US 95521461
```

Abstract (Basic): JP 6069515 A

Dwg.1/7

US 5818083 A

The semiconductor memory device includes an insulating **substrate** (1). A polycrystalline **semiconductor** layer (2) has is provided on the upper major surface of the insulating substrate. A **source region** (2a) is defined in the polycrystalline semiconductor layer. A **drain region** (2b) is defined in the polycrystalline semiconductor layer separated from the **source region**. The **source** and **drain regions** define between them a channel region as a part of the polycrystalline layer. A gate structure (7) is provided on the upper major **surface** of the polycrystalline **semiconductor** layer corresponding to the channel region.

The gate structure includes a **tunnelling** oxide **film** (3) provided on the upper major **surface** of the polycrystalline **semiconductor layer**. The **tunnelling** oxide **film** is **thick** enough to allow carriers to pass through it by a tunnelling effect. A **floating gate electrode** (4) provided on an upper major surface of the **tunnelling** oxide **film**. The **floating gate electrode** stores information in the form of electric charges. An intervening **insulation film** (5) is provided on an upper major surface of the **floating gate electrode**. A **control electrode** (6) is provided on an upper major surface of the intervening **insulation film**. The **tunnelling** oxide **film** directly contacts grains of the polycrystalline semiconductor layer.

USE - For **flash memory**.

ADVANTAGE - Increases storage **capacity**. Prevents deterioration or breakdown of **tunnelling** oxide **film**.

Dwg.1/10

29/3,AB/12 (Item 12 from file: 350)

DIALOG(R)File 350:Derwent WPIX

009804848

WPI Acc No: 1994-084703/199411

XRPX Acc No: N94-066301

Non-volatile semiconductor memory device for **flash memory** - has charge storage **electrode** and **control electrode** of larger width above isolation region than above channel region, in direction of cell column

Patent Assignee: MITSUBISHI DENKI KK (MITQ); MITSUBISHI ELECTRIC CORP (MITQ)

Inventor: AJIKA N; FUKUMOTO A; OHI M; ONODA H; KUNORI Y

Number of Countries: 003 Number of Patents: 004

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
DE 4327653	A1	19940310	DE 4327653	A	19930817	199411	B
JP 6077440	A	19940318	JP 92228552	A	19920827	199416	
US 5338957	A	19940816	US 93110151	A	19930823	199432	
DE 4327653	C2	20010419	DE 4327653	A	19930817	200122	

Priority Applications (No Type Date): JP 92228552 A 19920827

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
DE 4327653	A1		36	H01L-027/115	
JP 6077440	A		15	H01L-027/115	

US 5338957 A 36 H01L-029/68
DE 4327653 C2 H01L-027/115

Abstract (Basic): DE 4327653 A

The memory device consists of a substrate (1) with m x n cell charging electrodes (3) of 80-120 Angstroms **thick** polysilicon arranged in m lines, n columns. Two doped **regions** form **source** and **drain regions** directly beneath the electrode (3). An insulating area (4) of SiO2 is formed between each column across adjoining lines of electrodes (3).

A **control electrode** (6) is formed for each line. The width of electrodes (3,6) is set to be greater than insulating area (4) than over a channel area. This enhances the **capacitance** between electrodes (3,6).

ADVANTAGE - Improved coupling ratio allows lower voltage operation. Stepped region of connecting layer is reduced, and patterning process simplified.

Dwg.1/48

Abstract (Equivalent): US 5338957 A

The **nonvolatile semiconductor memory** device comprises a **semiconductor substrate** having a main surface, with mxn charge storage electrodes arranged in a matrix of m rows and n columns on the main surface of the substrate with a first **insulating film** between them. A pair of impurity **regions** serving as **source/drain regions**, are formed a predetermined distance apart on the main surface of the substrate to sandwich in the column direction a channel region formed directly beneath the charge storage electrode. An element isolation region is formed between each column across two adjacent columns of the charge storage electrode.

A number m **control electrodes** corresp. to each row are formed on the charge storage electrode with a second **insulating film** between them. The width in the column direction of the charge storage **electrode** and the **control electrode** above the element isolation region is set to be wider than the width in the column direction of the same above the channel region forming a wider area, so that in the wider area the charge storage **electrode** and the **control electrode** above the element isolation region protrude in opposite column directions w.r.t. the width of the electrodes above the channel region.

USE/ADVANTAGE - **Capacitance** between **control electrode** and charge storage electrode can be increased to improve coupling ratio in **nonvolatile memory**. Patterning of first interconnection layer can be carried out easily and precisely.

Dwg.1/48

29/3,AB/13 (Item 13 from file: 350)
DIALOG(R)File 350:Derwent WPIX

009702931
WPI Acc No: 1993-396484/199350
XRAM Acc No: C93-176470
XRPX Acc No: N93-306438

Fabricating high density contactless **EPROM** - with appropriate **capacitive coupling** between **control** and **floating gates**

Patent Assignee: SGS THOMSON MICROELTRN SRL (SGSA); SGS THOMSON MICROELTRN SARL (SGSA)

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Inventor: BELLEZZA O; CRISENZA G P; FONTANA G
Number of Countries: 007  Number of Patents: 006
Patent Family:
Patent No      Kind   Date      Applicat No     Kind   Date      Week
EP 573728       A1   19931215  EP 92830282      A    19920601  199350  B
JP 6188396      A    19940708  JP 93156098      A    19930601  199432
EP 573728       B1   19960103  EP 92830282      A    19920601  199606
DE 69207386     E    19960215  DE 607386        A    19920601  199612
                               EP 92830282      A    19920601
US 5707884      A    19980113  US 9370084       A    19930528  199809
                               US 95458059      A    19950601
US 5723350      A    19980303  US 9370084       A    19930528  199816

Priority Applications (No Type Date): EP 92830282 A 19920601
Patent Details:
Patent No  Kind Lan Pg   Main IPC     Filing Notes
EP 573728     A1 E  30 H01L-021/82
   Designated States (Regional): DE FR GB IT SE
JP 6188396    A     20 H01L-027/115
EP 573728     B1 E  33 H01L-021/82
   Designated States (Regional): DE FR GB IT SE
DE 69207386   E        H01L-021/82   Based on patent EP 573728
US 5707884    A     44 H01L-021/8247 Div ex application US 9370084
US 5723350    A     46 H01L-021/8247
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Abstract (Basic): EP 573728 A

A matrix of **floating gate** memory cells organised in rows and columns with bit lines in the form of diffused regions alternately continuous and contacted directly through a metal line and discontinuous and contacted through respective select transistors arranged along at least two rows of offset select transistors every certain number of rows of matrix's memory cells on a **semiconductor substrate** of first conductivity type, is obtd. by (a) forming pad oxide layer and defining and depositing a masking nitride layer; (b) forming field oxide defining channel regions in the form of parallel strips oriented along a first direction and rows of offset insular areas of select transistors and contacts of continuous bit lines; (c) removing masking nitride and pad oxide; (d) thermally growing gate oxide over channel and insular regions; (e) defining by masking the area of matrix of memory cells, etching gate oxide, and implanting a dopant of first type in the channel area, removing mask and growing **tunnel** oxide **layer** thinner than the partial **thickness** of the removed gate oxide while increasing the gate oxide in other areas; (f) depositing polycrystalline Si doped to a desired conductivity, forming ann interpoly **insulating multilayer protected** by polycrystalline Si and depositing silicon nitride to protect the Si from oxidn.; (g) masking the silicon nitride; (h) etching the silicon nitride, **protective** polycrystalline Si, interpoly **layer**, doped polycrystalline Si, gate or tunnel oxide and field oxide at crossings to expose the substrate along a plurality of alternately continuous and interrupted strips parallel to each other oriented orthogonally in respect to underlying strips of field oxide defining strip shaped channel regions withinn the area of the matrix of cells; (i) implanting a heavy dose of second type dopant in exposed areas of the substrate within the matrix area to form diffused bit lines each coinciding with either a **source** or **drain region** of a second type of conductivity of memory cells arranged along a same column; (j) diffusing the dopant and oxidising the surface while protecting the areas outside the memory cells from oxidation by the silicon nitride;

etc..

USE/ADVANTAGE - The method permits the fabrication of a contactless cross point definition matrix with a more comfortable pitch of bit line metal definition with an appropriate **capacitive coupling** between **control** and **floating gates.**

(Dwg.10/11

Abstract (Equivalent): EP 573728 B

A process of fabricating a matrix of **floating gate** memory cells organised in rows and columns, with bitlines in the form of diffused regions alternately - continuous and contacted directly through a metal line, and - discontinuous and contacted through respective select transistors, the select transistors being arranged along at least two offset rows which are provided every certain number of rows of matrix memory cells on a **semiconducting substrate** having a first type of conductivity and comprising the steps of forming a pad oxide layer (2) on the substrate (1), depositing and defining a masking nitride layer (3), forming a field oxide (4) defining channel regions of the cells in the form of parallel strips oriented along a first direction and rows of offset insular areas of the select transistors and of contacts of the continuous bitlines, removing the masking nitride and the pad oxide, thermally growing a layer of gate oxide (5) having a certain partial **thickness** over the channel regions and the insulator areas defined by the field oxide, defining by masking the area of the matrix of memory cells, etching the gate oxide and implanting a dopant of the first type of conductivity in the channel areas of the memory cells and removing the mask and growing a **layer** of **tunnel** oxide having a **thickness** smaller than the partial **thickness** of the removed gate oxide layer while increasing the **thickness** of the gate oxide layer in other areas, depositing a layer of polycrystalline silicon of first level and doping the polycrystalline silicon for increasing electrical conductivity to a desired value, forming an interpoly **insulating multilayer,** depositing a **protective layer** of polycrystalline silicon over the interpoly-**insulating multilayer** and depositing a layer of silicon nitride having a **thickness** capable of protecting from oxidn. the **protective layer** of polycrystalline silicon, masking the silicon nitride layer, etching the silicon nitride **layer** the **protective** polycrystalline silicon **layer,** the interpoly isolation multilayer, the doped polycrystalline silicon layer of first level, the gate or tunnel oxide and the field oxide at crossings until exposing the **semiconducting substrate** along a plurality of alternately continuous and interrupted strips parallel to each other and oriented orthogonally in respective to underlying strips of field oxide defining the strip-shaped channel regions, within the area occupied by the matrix of cells, implanting a heavy dose of a dopant capable of producing a second type of conductivity in exposed areas of the **semiconducting substrate** within the matrix area to form matrix's diffused bitlines, each coinciding either with **source** or with **drain regions** of a second type of conductivity of memory cells arranged along a same column, diffusing the implanted dopant and oxidising the **surface** of the **semiconducting substrate** in the areas exposed and implanted during the preceding steps while maintaining the other areas external to the area occupied by the memory cells protected from oxidn. by the **protecting** silicon nitride **layer,** planarising the surface by depositing a planarising **layer** of **dielectric** material and etching the planarising layer thereby continuing the etching to remove the silicon nitride **layer** and exposing the **protection layer** of polycrystalline silicon, masking the area occupied by the memory cells and eliminating the **protective** polysilicon silicon **layer** and the interpoly isolation multilayer from all the areas external to the area, implanting a dopant of the first type of conductivity for adjusting the threshold in the channel areas of the select transistors and of transistors of circuits external to the matrix of memory cells, through the doped polycrystalline silicon layer of first level and the gate oxide layer, depositing and doping a layer of polycrystalline silicon of second level, depositing a layer of tungsten silicide, masking the tungsten silicide layer to define the gate of transistors of the external circuits as well as of the select transistors and he **control gates** of the matrix of memory cells in the form of parallel strips oriented in the first direction, etching the tungsten silicide layer and the doped polycrystalline silicon layer of second level, arresting the etching on the field oxide or on the planarising **dielectric** material in areas external to the area of the matrix of memory cells and on the interpoly **insulation multilayer** within the matrix's area, masking the areas external to the matrix area, performing a self-aligned etching of the interpoly isolation multilayer and of the doped polysilicon layer of first level within the matrix's area, planarising the surface by depositing a **layer** of planarising **dielectric** material followed by etching and depositing an intermediate isolation **dielectric layer**, forming a plurality of contacts on each of the continuous bitlines disposed alternately to the interrupted bitlines and depositing and defining parallel lines of a metallisation layer over each of the plurality of contacts of the continuous bitlines.

(Dwg.1/11

Abstract (Equivalent): US 5723350 A

A matrix of **floating gate** memory cells organised in rows and columns with bit lines in the form of diffused regions alternately continuous and contacted directly through a metal line and discontinuous and contacted through respective select transistors arranged along at least two rows of offset select transistors every certain number of rows of matrix's memory cells on a **semiconductor substrate** of first conductivity type, is obtd. by (a) forming pad oxide layer and defining and depositing a masking nitride layer; (b) forming field oxide defining channel regions in the form of parallel strips oriented along a first direction and rows of offset insular areas of select transistors and contacts of continuous bit lines; (c) removing masking nitride and pad oxide; (d) thermally growing gate oxide over channel and insular regions; (e) defining by masking the area of matrix of memory cells, etching gate oxide, and implanting a dopant of first type in the channel area, removing mask and growing **tunnel** oxide **layer** thinner than the partial **thickness** of the removed gate oxide while increasing the gate oxide in other areas; (f) depositing polycrystalline Si doped to a desired conductivity, forming ann interpoly **insulating multilayer protected** by polycrystalline Si and depositing silicon nitride to protect the Si from oxidn.; (g) masking the silicon nitride; (h) etching the silicon nitride, **protective** polycrystalline Si, interpoly **layer**, doped polycrystalline Si, gate or tunnel oxide and field oxide at crossings to expose the substrate along a plurality of alternately continuous and interrupted strips parallel to each other oriented orthogonally in respect to underlying strips of field oxide defining strip shaped channel regions withinn the area of the matrix of cells; (i) implanting a heavy dose of second type dopant in exposed areas of the substrate within the matrix area to form diffused bit lines each coinciding with either a **source** or **drain region** of a second type of conductivity of memory cells arranged along a same column; (j) diffusing the dopant and oxidising the surface while protecting the areas outside the memory cells from oxidation by the silicon nitride; etc..

USE/ADVANTAGE - The method permits the fabrication of a contactless cross point definition matrix with a more comfortable pitch of bit line metal definition with an appropriate **capacitive coupling** between **control** and **floating gates.**

Dwg.0/11

US 5707884 A

A matrix of **floating gate** memory cells organised in rows and columns with bit lines in the form of diffused regions alternately continuous and contacted directly through a metal line and discontinuous and contacted through respective select transistors arranged along at least two rows of offset select transistors every certain number of rows of matrix's memory cells on a **semiconductor substrate** of first conductivity type, is obtd. by (a) forming pad oxide layer and defining and depositing a masking nitride layer; (b) forming field oxide defining channel regions in the form of parallel strips oriented along a first direction and rows of offset insular areas of select transistors and contacts of continuous bit lines; (c) removing masking nitride and pad oxide; (d) thermally growing gate oxide over channel and insular regions; (e) defining by masking the area of matrix of memory cells, etching gate oxide, and implanting a dopant of first type in the channel area, removing mask and growing **tunnel** oxide **layer** thinner than the partial **thickness** of the removed gate oxide while increasing the gate oxide in other areas; (f) depositing polycrystalline Si doped to a desired conductivity, forming ann interpoly **insulating multilayer protected** by polycrystalline Si and depositing silicon nitride to protect the Si from oxidn.; (g) masking the silicon nitride; (h) etching the silicon nitride, **protective** polycrystalline Si, interpoly **layer,** doped polycrystalline Si, gate or tunnel oxide and field oxide at crossings to expose the substrate along a plurality of alternately continuous and interrupted strips parallel to each other oriented orthogonally in respect to underlying strips of field oxide defining strip shaped channel regions withinn the area of the matrix of cells; (i) implanting a heavy dose of second type dopant in exposed areas of the substrate within the matrix area to form diffused bit lines each coinciding with either a **source** or **drain region** of a second type of conductivity of memory cells arranged along a same column; (j) diffusing the dopant and oxidising the surface while protecting the areas outside the memory cells from oxidation by the silicon nitride; etc..

USE/ADVANTAGE - The method permits the fabrication of a contactless cross point definition matrix with a more comfortable pitch of bit line metal definition with an appropriate **capacitive coupling** between **control** and **floating gates.**

Dwg.0/11

29/3,AB/14 (Item 14 from file: 350)
DIALOG(R)File 350:Derwent WPIX

009254943
WPI Acc No: 1992-382360/199246
Related WPI Acc No: 1991-215366; 1991-238241; 1993-295237
XRPX Acc No: N92-291546

Single transistor **non-volatile** electrically alterable

memory device - has **floating gate** positioned between **control gate** and source and drain with **capacitive coupling** to source

Patent Assignee: SILICON STORAGE TECHNOLOGY INC (SILI-N); NOISE CANCELLATION TECHNOLOGIES (NOIS-N)

Inventor: WANG P; YEH B

Number of Countries: 018 Number of Patents: 007

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
WO 9218980	A1	19921029	WO 92US2194	A	19920313	199246	B
EP 579779	A1	19940126	EP 92917322	A	19920313	199404	
			WO 92US2194	A	19920313		
JP 6506798	W	19940728	JP 92510197	A	19920313	199434	
			WO 92US2194	A	19920313		
US 5572054	A	19961105	US 90467907	A	19900122	199650	
			US 91682459	A	19910409		
			US 94246574	A	19940520		
			US 95523037	A	19950901		
EP 579779	B1	19980708	EP 92917322	A	19920313	199831	
			WO 92US2194	A	19920313		
DE 69226176	E	19980813	DE 626176	A	19920313	199838	
			EP 92917322	A	19920313		
			WO 92US2194	A	19920313		
CA 2107676	C	20001031	CA 2107676	A	19920313	200060	
			WO 92US2194	A	19920313		

Priority Applications (No Type Date): US 91682459 A 19910409; US 90467907 A 19900122; US 94246574 A 19940520; US 95523037 A 19950901

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
WO 9218980	A1	E	40	G11C-013/00	
Designated States (National): CA JP					
Designated States (Regional): BE CH DE DK ES FR GB GR IT LI LU MC NL SE					
EP 579779	A1	E	2	G11C-013/00	Based on patent WO 9218980
Designated States (Regional): AT BE CH DE DK ES FR GB GR IT LI LU MC NL SE					
JP 6506798	W		13	H01L-029/788	Based on patent WO 9218980
US 5572054	A		19	H01L-029/68	CIP of application US 90467907 Cont of application US 91682459 Cont of application US 94246574 CIP of patent US 5029130
EP 579779	B1	E		G11C-013/00	Based on patent WO 9218980
Designated States (Regional): AT BE CH DE DK ES FR GB GR IT LI LU MC NL SE					
DE 69226176	E			G11C-013/00	Based on patent EP 579779 Based on patent WO 9218980
CA 2107676	C	E		G11C-011/404	Based on patent WO 9218980

Abstract (Basic): WO 9218980 A

The device comprising a single transistor non-volatile electrically alterable semi-conductor memory cell has a source (14), a drain (16) with a channel region (18), disposed on a substrate and **insulated** by a **layer** of silicon dioxide or nitride (20). A **floating gate** (22) is positioned partly over both channel and **source regions** and is **insulated** from the control **gate** (29) by an **insulating layer** (25).

In operation, when erasure is desired, a ground potential is applied to the source and drain, whilst a high positive voltage (+15 volts) is applied to the **control gate.** Charges on the **floating gate** are induced by the Fowler-Nordheim mechanism to **tunnel** through the **insulating layer** to the **control gate** leaving the **floating gate** positively charged.

ADVANTAGE - High efficiency in hot electron generation and injection onto **floating gate**, providing for very low levels of programming current.

Dwg.1/4

Abstract (Equivalent): US 5572054 A

A method of programming a select storage site from an electrically programmable and erasable memory array device having a plurality of interconnected storage sites, while minimizing programming disturbance on a plurality of non-selected storage site in said array, said device having a **substrate** of **semiconductor** material of a first conductivity type, with each storage site including a single asymmetrical transistor, with each transistor having first and second spaced-apart regions in said substrate with a channel region therebetween, said first and second regions are of a second conductivity type; a first **insulating layer** disposed over said substrate including over said first, second and channel regions; an electrically conductive **floating gate** disposed over said first **insulating layer** and extending over a portion of said channel region and over a portion of said second region to maximize a **capacitive coupling** therewith; a second **insulating layer** disposed over and adjacent said **floating gate** and having a **thickness** permitting Fowler-Nordheim tunneling of charges therethrough; an electrically conductive **control gate** having two electrically connected sections, a first section disposed over said first **insulating layer**, spaced apart from said **floating gate** and adjacent to said second **insulating layer**, extending over a portion of said first region; said second section disposed over said second **insulating** layer to minimize **capacitive coupling** with said **floating gate**; said method comprising:

applying a first positive potential to the second region of each transistor of all the storage sites including said select storage site and said plurality of non-selected storage sites;

applying a ground potential to the first region of each transistor of a first plurality of the storage sites, said first plurality being less than all of the storage sites but including at least said select storage site and excluding said plurality of non-selected storage sites;

applying a second positive potential, less than the first positive potential, to the **control gate** of each transistor of a second plurality of storage sites, said second plurality being less than all of the storage sites and having at least said select storage site in common with said first plurality and at least a first of said plurality of non-selected storage sites;

applying a third positive potential, less than the first positive potential but greater than the second positive potential, to the first region of the plurality of transistors at the non-selected storage sites; and

whereby the transistor at the select storage site in said first plurality in common with said second plurality is programmed, and said programming disturbance on said plurality of non-selected storage sites is minimized.

(Dwg.2/4-S

- 3

29/3,AB/15 (Item 15 from file: 350)

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DIALOG(R)File 350:Derwent WPIX
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009166919
WPI Acc No: 1992-294353/199236
Related WPI Acc No: 1996-478993
XRPX Acc No: N92-225505
  Transistor structure used in erasable and programmable memories - has
  semiconductor with source, channel and DRAM with floating
  polysilicon@ gate extending over oxide layer forming
  capacitor
Patent Assignee: INTERUNIVERSITAIR MICRO-ELEKTRONICA (INTE-N);
  INTERUNIVERSITAIR MICROELECTRONICA CENT (INTE-N); INTERUNIV
  MICROELEKTRONICA CENT VZW (INTE-N); INTERUNIV MICRO-ELECTRONICA CENT VZW
  (INTE-N)
Inventor: GROESENEKEN G; MAES H; VAN HOUDT J
Number of Countries: 017 Number of Patents: 010
Patent Family:
Patent No      Kind   Date     Applicat No    Kind   Date     Week
EP 501941       A1  19920902  EP 92870016     A   19920130  199236  B
BE 1004424      A3  19921117  BE 9191         A   19910131  199302
JP 5082794      A   19930402  JP 9240114      A   19920130  199318
EP 501941       B1  19961023  EP 92870016     A   19920130  199647
DE 69214688     E   19961128  DE 614688       A   19920130  199702
                              EP 92870016     A   19920130
US 5583810      A   19961210  US 92827715     A   19920129  199704
                              US 9380225      A   19930621
US 5583811      A   19961210  US 92827715     A   19920129  199704
                              US 9380225      A   19930621
                              US 94275016     A   19940713
ES 2095453      T3  19970216  EP 92870016     A   19920130  199714
JP 3236054      B2  20011204  JP 9240114      A   19920130  200203
KR 280051       B   20010201  KR 921333       A   19920130  200211

Priority Applications (No Type Date): BE 9191 A 19910131
Patent Details:
Patent No  Kind Lan Pg   Main IPC     Filing Notes
EP 501941     A1 E   9 H01L-029/788
   Designated States (Regional): AT BE CH DE DK ES FR GB GR IT LI NL PT SE
BE 1004424    A3 F  10 H01L-000/00
JP 5082794    A        H01L-029/788
EP 501941     B1 E   9 H01L-029/788
   Designated States (Regional): AT BE CH DE DK ES FR GB GR IT LI NL PT SE
DE 69214688   E        H01L-029/788  Based on patent EP 501941
US 5583810    A     13 G11C-016/04   CIP of application US 92827715
US 5583811    A     13 G11C-016/04   CIP of application US 92827715
                                     Cont of application US 9380225
ES 2095453    T3       H01L-029/788  Based on patent EP 501941
JP 3236054    B2     8 H01L-021/8247 Previous Publ. patent JP 5082794
KR 280051     B        H01L-027/10   Previous Publ. patent KR 92015561

Abstract (Basic): EP 501941 A
        The structure comprises a semiconductor substrate
    including a source region and a channel and drain
    region. A floating polysilicon gate (16) extends over
    a portion of the channel with an oxide layer (15) between. The
    floating gate (16) has an extension (18) which is insulated
    from the semiconductor substrate (11). A control
    gate (17) extends over a portion of the floating gate
    (16) from above the source region.
```

It extends to the **drain region** through a **dielectric** oxide **layer** to form a **capacitor** with **floating gate** extension, program **gate** (19) and **control gate** (17) having lateral edges facing each other.

ADVANTAGE - Can be manufactured using standard CMOS technology.

Dwg.3/9

Abstract (Equivalent): EP 501941 B

A **non-volatile semiconductor memory** device, comprising a **semiconductor substrate** (11) of a first conductivity type, having a **source region** (12) and a **drain region** (14) of a second conductivity type which define a channel region (13) in an active area (10) therebetween, a polysilicon **floating gate** (16) extending over a portion of said channel **region** at the **drain** side of the device and being insulated from said channel region (13) by a thin oxide layer (15), and a polysilicon **control gate** (17) extending over a portion of said channel at the source side of the device and extending over a portion of said **floating gate** (16) **insulated** therefrom by a **dielectric layer,** characterised in that: said **floating gate** has an extension (18) extending outside said channel region (13) in a direction perpendicular to the channel length direction, said extension (18) being insulated from the silicon substrate (11) by a **thick** oxide layer (22), and having a sufficient length to form a **capacitor** outside the channel region; the memory device further comprises a program gate (19) extending over said **floating gate** extension (18) and being **insulated** therefrom by a **dielectric layer** so as to form a **capacitor** with said **floating gate** extension, said **capacitor** being large enough to couple a voltage to the **floating gate** (16); and said **control gate** (17) and said program gate (19) have lateral edges that are facing each other in a spaced apart relationship.

(Dwg.1/9

Abstract (Equivalent): US 5583810 A

A method of programming a **floating gate** transistor, said transistor comprising a **semiconductor substrate** including a **source region**, a **drain region** and a channel extending between said **source** and **drain regions**, a **floating gate** extending over a portion of said channel and ending over said channel, said **floating gate** integrally including first and second **floating gate** portions, said first **floating gate** portion extending proximately to said channel with a thin oxide layer therebetween and said second **floating gate** portion extending away from said channel, a program gate **capacitively coupled** through a **dielectric** oxide **layer** to said second **floating gate** portion, and a **control gate** laterally remote from said program gate and extending through a **dielectric** oxide **layer** over said first **floating gate** portion from above said **source region** to above said **drain region**, said program **gate** and said **control gate** having lateral edges facing each other in a spaced apart relationship, said method comprising the steps of:

applying a high voltage to said program gate thereby **capacitively coupling** a high voltage to said second **floating gate** portion;

applying a low voltage to said **control gate;** and

applying a voltage not greater than 5 V to said **drain region**, to thereby cause a very high hot-electron injection towards said **floating gate** while achieving, within a microsecond, a programming of said transistor without the need for an external voltage supply.

(Dwg.2,3/12)

US5583811 A programmable **EEPROM** cell structure for use as an erasable programmable semiconductor memory device, comprising:

a **semiconductor substrate** including a **source region**, a **drain region** and a channel extending between said **source** and **drain regions,** with a **drain** voltage between said **source** and **drain regions;**

a **floating gate** extending over a portion of the channel with a thin oxide layer therebetween;

a **control gate** extending over a portion of said **floating gate** from above said **source region** to above said **drain region** through a **dielectric** oxide **layer;** and

a program **gate** extending above said **floating gate** with a **dielectric** oxide **layer** therebetween, said program gate forming a **capacitor** with said **floating gate** with a coupling ratio sufficient to couple a voltage at least as high as said drain voltage to said **floating gate,** thereby establishing a high voltage at a point in said channel between said **control gate** and said **floating gate** and ensuring a high hot-electron injection towards said **floating gate.**

(Dwg.2,3/1
2)

US 5583811 A

A programmable **EEPROM** cell structure for use as an erasable programmable semiconductor memory device, comprising:

a **semiconductor substrate** including a **source region**, a **drain region** and a channel extending between said **source** and **drain regions,** with a **drain** voltage between said **source** and **drain regions;**

a **floating gate** extending over a portion of the channel with a thin oxide layer therebetween;

a **control gate** extending over a portion of said **floating gate** from above said **source region** to above said **drain region** through a **dielectric** oxide **layer;** and

a program **gate** extending above said **floating gate** with a **dielectric** oxide **layer** therebetween, said program gate forming a **capacitor** with said **floating gate** with a coupling ratio sufficient to couple a voltage at least as high as said drain voltage to said **floating gate,** thereby establishing a high voltage at a point in said channel between said **control gate** and said **floating gate** and ensuring a high hot-electron injection towards said **floating gate.**

Dwg.2,3/12

29/3,AB/16 (Item 16 from file: 350)
DIALOG(R)File 350:Derwent WPIX

008526740

WPI Acc No: 1991-030824/199105
XRAM Acc No: C91-013152
XRPX Acc No: N91-023861

Re-programmable **nonvolatile semiconductor** device - can be miniaturised and has a large **capacity**

Patent Assignee: TOSHIBA KK (TOKE)
Inventor: YOSHIKAWA K
Number of Countries: 006 Number of Patents: 007
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
EP 410424	A	19910130	EP 90114270	A	19900725	199105	B
JP 3055880	A	19910311	JP 89191839	A	19890725	199116	
US 5015601	A	19910514	US 90553592	A	19900718	199122	
US 5159431	A	19921027	US 90433592	A	19900718	199246	
			US 91654687	A	19910213		
KR 9309139	B1	19930923	KR 9011036	A	19900720	199436	
EP 410424	B1	19941005	EP 90114270	A	19900725	199438	
DE 69013094	E	19941110	DE 613094	A	19900725	199444	
			EP 90114270	A	19900725		

Priority Applications (No Type Date): JP 89191839 A 19890725
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 410424	A				
Designated States (Regional): DE FR GB					
US 5159431	A		8	H01L-029/34	Div ex application US 90433592 Div ex patent US 5015601
EP 410424	B1	E	11	H01L-029/788	
Designated States (Regional): DE FR GB					
DE 69013094	E			H01L-029/788	Based on patent EP 410424
KR 9309139	B1			H01L-027/115	

Abstract (Basic): EP 410424 A

Nonvolatile semiconductor device is made up of several semiconductor elements each of which comprises a **semiconductor substrate** of a first conductivity type; **source** and **drain regions** formed in a surface region of the substrate and having a second type conductivity; a first **gate electrode** formed above a channel **region** between **source** and **drain regions**, and kept in an electrically-floating state by a first gate **insulation film** ; a second gate **electrode** serving as a **control gate**, and formed above first gate **electrode** with a second gate **insulation film** interposed.

The **source** and **drain regions** are formed under a third **insulation film, thicker** than the first **gate insulation film**, and which isolates the channel region of one semiconductor element from that of an adjacent one; sepd. from each other at a position corresp. to an end portion of the first **gate electrode.**

USE/ADVANTAGE - For mfr. of a **nonvolatile memory**, e.g. **EPROM**, which can be miniaturised and has a large **capacity**.

(10pp Dwg.No.7/8)

Abstract (Equivalent): EP 410424 B

A **non-volatile semiconductor memory** device made up of a plurality of memory cells arranged in rows and columns, each of which comprises: a **semiconductor substrate** (101) of a first conductivity type; a **source region** (104) and a **drain region** (102) which are formed in a **surface** region of the **semiconductor substrate** (101) and have a second conductivity type and define the row direction; a first

gate electrode (108) formed above a channel **region** (105) between the **source** and **drain regions** (104, 102) and kept in an electrically-floating state by a first **gate insulation film** (107); and a second **gate electrode** (110) serving as a **control gate** and formed above the first **gate electrode** (108), with a second **gate insulation film** (109) interposed, said **source** and **drain regions** (104, 102) being formed under adjacent third **insulation films** (106) which are **thicker** than the first **gate insulation film** (107) and which isolate the channel region (105) of one memory cell from that of an adjacent one with the same row, characterized in that **source** and **drain regions** of adjacent cells within the same row (104, 102) being located under the same third **insulation film** (106) and separated from each other at a position corresponding to an end portion of the first **gate electrode** (108).

Dwg.7/8

Abstract (Equivalent): US 5159431 A

A **nonvolatile semiconductor** device has a **semiconductor substrate** with a source and drain in the substrate defining a channel region. An **insulation film** is applied and a **gate electrode** in an electrically **floating** state positioned above the channel and covered by a second **insulating film.** A **control gate** is formed above the **gate electrode** and covered by a third (**thicker) insulation film.**

A trench is formed between the source of one semiconductor element and the **drain region** of an adjacent element. The trench being filled by a third **insulation film.** The trench serving to electrically isolate adjacent channels and the **source** and **drain regions** of adjacent semiconductor elements.

ADVANTAGE - Devices can be miniaturised while retaining high **capacity**.

Dwg.1/8

US 5015601 A

The method comprises (a) forming embedded layers of 2nd type in a 1st type substrate, (b) forming an channel region between the embedded layers by ion implantation and then forming a 1st **gate insulation film** on the channel region, (c) forming an **insulation film thicker** than the 1st **insulation film**, (d) forming a 1st **gate electrode** above the channel region such that the 1st **gate electrode** is kept in an electrically floating condition, (e) forming a trench extending through the **insulating film** and the embedded layer and reacting the substrate interior, thus dividing the embedded layer into **source** and **drain regions,** (f) filling the trench with an insulating material, insulating and isolating adjacent elements from each other, (g) forming a 2nd **insulation film**, and (h) forming a 2nd gate **electrode** on the 1st **gate** electrode, the **insulation film** and the trench to electrically connect one element to the adjacent one.

USE/ADVANTAGE - Used to mfr. a reprogrammable nonvolatile device such as an **EPROM,** which can be miniaturised and have a large **capacity.** (8pp)

29/3,AB/17 (Item 17 from file: 350)
DIALOG(R)File 350:Derwent WPIX

008129121
WPI Acc No: 1990-016122/199003
Related WPI Acc No: 1990-260536; 1991-008556; 1992-131549; 1992-424278
XRAM Acc No: C90-006910
XRPX Acc No: N90-012386

EEPROM with self aligned tunnel window - has reduced cell size and improved coupling between **control gate** and **floating gate**

Patent Assignee: TEXAS INSTR INC (TEXI); TEXAS INSTR CORP (TEXI)
Inventor: GILL M; LIN S W; CLEAVELIN C R; LIN S; MCELROY D J
Number of Countries: 008 Number of Patents: 008
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
EP 350771	A	19900117	EP 89112200	A	19890704	199003	B
JP 2161778	A	19900621	JP 89183540	A	19890715	199031	
US 5008721	A	19910416	US 90494042	A	19900315	199118	
US 5155055	A	19921013	US 88219529	A	19880715	199244	
			US 90494042	A	19900315		
			US 91685358	A	19910415		
EP 350771	A3	19920902	EP 89112200	A	19890704	199338	
EP 350771	B1	19941012	EP 89112200	A	19890704	199439	
DE 68918771	E	19941117	DE 618771	A	19890704	199445	
			EP 89112200	A	19890704		
KR 139806	B1	19980715	KR 8910151	A	19890715	200018	

Priority Applications (No Type Date): US 88219529 A 19880715; US 90494042 A 19900315; US 91685358 A 19910415
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 350771	A	E	6		
Designated States (Regional): DE FR GB IT NL					
US 5008721	A		9		
US 5155055	A		10	H01L-021/76	Cont of application US 88219529 Div ex application US 90494042 Div ex patent US 5008721
EP 350771	B1	E	12	H01L-029/788	
Designated States (Regional): DE FR GB IT NL					
DE 68918771	E			H01L-029/788	Based on patent EP 350771
KR 139806	B1			G11C-008/00	

Abstract (Basic): EP 350771 A

An **EEPROM** is constructed to have a **floating-gate** (17) with a small self-aligned tunnel window (19) located on the opposite side of the source (15) from the channel and drain (16). The device has a contact-free cell (10) layout, and the bit lines (13) and **source/drain regions** (15,16) in this cell (10) are buried beneath relatively **thick** silicon oxide. The tunnel window (19) has a thinner **dielectric** (20) than the rest of the **floating gate** (17) to facilitate tunneling of electrons. The method of mfr. of the device is claimed.

USE/ADVANTAGE - The self-aligned tunnel simplifies mfr. and so enhances reliability, and the contact free cell layout permits reduced cell size. Use of a **thick** silicon oxide layer over the bit lines and **source/drain regions** gives a favourable ratio of **control gate** to **floating gate capacitance**, The cell is resistant to bit line stress and has improved field-plate breakdown voltage. A single low-voltage external supply can be used for both programming and erasing, so that the memory is compatible with on-board programming in systems with a single external power supply.

Abstract (Equivalent): EP 350771 B

An **EEPROM** is constructed to have a **floating-gate** (17) with a small self-aligned tunnel window (19) located on the opposite side of the source (15) from the channel and drain (16). The device has a contact-free cell (10) layout, and the bitlines (13) and **source/drain regions** (15,16) in this cell (10) are buried beneath relatively **thick** silicon oxide. The tunnel window (19) has a thinner **dielectric** (20) than the rest of the **floating gate** (17) to facilitate tunneling of electrons. The method of mfr. of the device is claimed.

USE/ADVANTAGE - The self-aligned tunnel simplifies mfr. and so enhances reliability, and the contact free cell layout permits reduced cell size. Use of a **thick** silicon oxide layer over the bitlines and **source/drain regions** gives a favourable ratio of **control gate** to **floating gate capacitance** , The cell is resistant to bitline stress and has improved field-plate breakdown voltage. A single low-voltage external supply can be used for both programming and erasing, so that the memory is compatible with on-board programming in systems with a single external power supply.

EP-350771 An electrically-erasable, electrically-programmable, **floating-gate** memory cell (10), comprising: a **source region** (14) and a **drain region** (16) formed in a face of a semiconductor body (11), each of said regions (15, 16) being heavily-doped and of conductivity-type opposite that of underlying material of said body (11), each of said regions (15, 16) being buried under a layer of silicon oxide on said face, said **source region** (15) being spaced from said **drain region** (16) on said face by a channel area, a **floating gate** (17) over at least a part of said channel area and extending onto said silicon oxide layer over the **source region** (15), the **floating gate** (17) being separated from the channel area of said face by a **gate insulator** (20), a **tunnel** area (19) adjacent said **source region** (15) but on the opposite side of said **source region** (15) from said channel area, said **floating gate** (17) also extending over said tunnel area (19) and being separated from said tunnel area (19) by a **tunnel insulator**, the **thickness** of said **tunnel insulator** at said **tunnel** area being much less than the **thickness** of said **gate insulator** (20) at the channel area, and a **control gate** (12) extending along said face over said **floating gate** (17) and over said **source** and **drain regions** (15, 16), said **control gate** (12) being separated from said **floating gate** (17) by an **insulator coating** (34) characterizzed in that said silicon oxide layer is much **thicker** than said **gate insulator** (20) at said channel area.

(Dwg.1/4

Abstract (Equivalent): US 5155055 A

An array of non-volatile rows and columns of memory cells on the face of a **semiconductor surface** is formed by initially forming multiple separated insulator regions between which the bit lines are formed. Each bit line having **source** and **drain regions**. A second **insulator layer** with sloping lateral edges is formed on each bit **layer**. An **insulator layer** is also formed over each channel of the cell. The insulation is removed above each **source** and **drain region** before forming a **tunnel** window **insulator** on the exposed portion of the surface. ADVANTAGE - By allowing the tunnel window to be thinner than the rest of the **insulating layer** Fowler-Nordheim **tunnelling** is enhanced. The process provides self-alignment of the tunnel. (Dwg.2A/4)

US 5008721 A

Memory cell, formed at a face of a semiconductor layer (I) of a first conductivity type, comprises a) a **thick** insulator region selectively grown at the face of (I), a lateral margin of a) sloped w.r.t. the face, a) having a **thickness;** b) first and second **source/drain regions** implanted into the face with a dopant to be of a second conductivity type opposite the first conductivity type; c) an oxide region grown on the first **source/drain region,** a lateral margin of c) being sloped w.r.t. the face, c) having a **thickness,** a junction of the sloped lateral margin of c), and the sloped lateral margin of a), creating a thin insulator transition area, adjoining the first **source/drain region;** d) insulator material within the thin insulator transition area etched back to expose (I), a thin **tunnel insulator** grown on the exposed layer (I) within the thin transition area, a width of the insulator between a) and c), being independent of the **thicknesses** of a) and c); e) a channel area of (I) extending between the first and second **source drain regions,** a **floating gate** formed over the **tunnel insulator** and **insulatively** over at least part of area e); and f) a **control gate insulatively** adjacent the **floating gate.** USE - New cell is electrically erasable and programmable. (9pp)

29/3,AB/18   (Item 18 from file: 350)
DIALOG(R)File 350:Derwent WPIX

007800546
WPI Acc No: 1989-065658/198909
XRAM Acc No: C90-051063
XRPX Acc No: N90-090064

Non-volatile semiconductor memory device - has MOS transistor memory cell voltage applied between two gates to inject or take out electrons from intermediate gate

Patent Assignee: OKI ELECTRIC IND CO LTD (OKID)
Number of Countries: 003 Number of Patents: 003
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
JP 1018270	A	19890123	JP 87174543	A	19870713	198909	B
US 4907197	A	19900306	US 88218303	A	19880712	199016	
KR 9612167	B1	19960916	KR 888710	A	19880713	199925	

Priority Applications (No Type Date): JP 87174543 A 19870713
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
JP 1018270	A		4		
US 4907197	A		13		
KR 9612167	B1			H01L-027/10	

Abstract (Basic): US 4907197 A

A one-transistor, **floating gate, non-volatile memory** cell (10) consists of an MOS transistor on a **semiconductor substrate** (11) which comprises a channel **region** between **source** (12) and drain (13), a first **dielectric** surface **layer** on which is a select gate (14) overlying part of the channel region, with one end being adjacent to the source, and an injection gate (16) over part of the channel region, with one end adjacent to the source, and an injection gate (16) over part of the channel region, with one end being adjacent to the drain. A second **dielectric layer** is formed on the first and the gates, and on this is formed a **floating gate** (15) so that it has a larger **capacitance** with the select gate than with the injection gate, with the middle region of the **floating gate** being between the ends of the other gates in order to achieve this aim.

Also claimed is a memory device comprising a plurality of memory cells as above but with each MOS transistor additionally comprising a third **dielectric layer** on the second and **floating gate**, a contact hole (18) through all three **dielectric layers** to expose the drain, a contact hole through the second and third layers to expose the select gate, a bit line on the third **dielectric layer** and in the first contact hole to contact the drain, and a word line on this layer and in the second contact hole to contact the select gate.

USE/ADVANTAGE - A **non-volatile semiconductor memory** device (claimed) of the **floating gate EEPROM** type, with smaller cell size and with good control of the **thickness** and properties of the **tunnel** oxide **film,** is provided. The process of mfr. is relatively simple and uses existing procedures. (First major country equivalent to J01018270-A). (13pp Dwg.No.1/9)

29/3,AB/19 (Item 1 from file: 347)
DIALOG(R)File 347:JAPIO
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05645715
NONVOLATILE SEMICONDUCTOR STORAGE DEVICE AND ITS MANUFACTURE

PUB. NO.: 09-260515 [JP 9260515 A]
PUBLISHED: October 03, 1997 (19971003)
INVENTOR(s): KONDO HIROSHI
APPLICANT(s): RICOH CO LTD [000674] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 08-090060 [JP 9690060]
FILED: March 18, 1996 (19960318)

ABSTRACT

PROBLEM TO BE SOLVED: To increase the overlapping area of a **control gate electrode** and a **source region** or the **drain region,** by forming the **source region** and a **drain region** in a slf-alignment manner, without decreasing a **capacitive coupling** ratio.

SOLUTION: On a channel **region** between a **source region** 6 and a **drain region** 7 of a **semiconductor substrate** 1, a **floating gate electrode** 3 is formed via a first **insulating film** 2, and a **control gate electrode** 5 extending in the channel width direction is formed via a second **insulating film** 4. The width of the **floating gate electrode** 3 in the channel length direction is set equal to that of the **control gate electrode** 5 in the same direction. The **source region** 6 and the **drain region** 7 exist as far as the under part of the **floating gate electrode** 3, and partly overlap with it. As a result, the **thickness** of the side part region in the channel length direction of

the **control gate electrode** 5 is less than. the **thickness** of the central part. The voltage of the **control gate electrode** necessary for writing erasing can be reduced.

29/3,AB/20 (Item 2 from file: 347)
DIALOG(R)File 347:JAPIO
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03152977
NONVOLATILE MEMORY DEVICE

PUB. NO.: 02-128477 [JP 2128477 A]
PUBLISHED: May 16, 1990 (19900516)
INVENTOR(s): NAKAYAMA RYOZO
SHIRATA RIICHIRO
KIRISAWA RYOHEI
ARITOME SEIICHI
ENDO TETSUO
MASUOKA FUJIO
APPLICANT(s): TOSHIBA CORP [000307] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 63-280291 [JP 88280291]
FILED: November 08, 1988 (19881108)
JOURNAL: Section: E, Section No. 960, Vol. 14, No. 362, Pg. 99, August 06, 1990 (19900806)

ABSTRACT

PURPOSE: To obtain a memory free from an erroneous readout by a method wherein a **floating gate** is formed on the center of the **surface** of a **semiconductor substrate** through the intermediary of a **tunnel** oxide **film,** a **control gate** is provided thereon through the intermediary of an **insulating film** , and ions are implanted slantingly into a part of the substrate at both the sides of the gates using these gate as a mask.

CONSTITUTION: A **tunnel** oxide **film** 2 of a specified size 40-150 angstroms in **thickness** is formed on the center of the surface of an Si substrate 1, and a **floating gate** 3 is provided thereon. And, a **control gate** 5 is formed thereon through the intermediary of an **insulating film** 4, and ions are implanted to form a **source region** 6 and a **drain region** 7 in a part of the substrate at both the sides of the **control gate** 5 using these gates as mask. The ion implantation is executed in such a manner that they are implanted in a certain direction slanting by 5 degrees to the vertical line and the end of the **source region** 6 is made to slip under the gate 5 and the **drain region** 7 is separated from the end of the gate 5 to make a junction **capacitance** small. By this setup, even if readout increase in times, a threshold can be made to fluctuate hardly and an erroneous readout can be prevented.

29/3,AB/21 (Item 3 from file: 347)
DIALOG(R)File 347:JAPIO
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03052273
MANUFACTURE OF **NONVOLATILE SEMICONDUCTOR MEMORY**

PUB. NO.: 02-027773 [JP 2027773 A]

PUBLISHED: January 30, 1990 (19900130)
INVENTOR(s): YAMAGATA YASUJI
APPLICANT(s): NEC CORP [000423] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 63-177411 [JP 88177411]
FILED: July 15, 1988 (19880715)
JOURNAL: Section: E, Section No. 913, Vol. 14, No. 170, Pg. 155, March 30, 1990 (19900330)

ABSTRACT

PURPOSE: To improve insulating characteristic between a **control gate electrode** and a **floating gate** by forming an oxide film having a **thickness** of sufficient insulating characteristic on the side face of the **floating gate**, and forming a multilayer structure of an oxide film, a nitride **film** having high **coupling capacity** value between the **floating gate** and the **control gate** on the upper surface of the **floating gate**.

CONSTITUTION: A first gate oxide film 3 is formed on one conductivity type **semiconductor substrate** 1, and a **floating gate electrode** 8 made of polycrystalline silicon and a second **gate insulating film** 9 having a silicon oxide film and a silicon nitride film are formed on the film 3. With the film 9 as a mask a silicon oxide film 11 is formed on the side face of the **electrode** 8. A **control gate electrode** 16 is formed from part of the electrode 8 to the substrate. With the electrodes 16, 8 as masks a **drain region** 17 and a **source region** are formed.

33/3,AB/1 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX

015149133
WPI Acc No: 2003-209660/200320
Related WPI Acc No: 2002-255582; 2004-293258
XRAM Acc No: C03-053360
XRPX Acc No: N03-167157
Non-volatile semiconductor memory device
comprises **control gate** on **semiconductor substrate**
in which device active area and device isolation area are defined
Patent Assignee: HYNIX SEMICONDUCTOR INC (HYNI-N)
Inventor: KIM H
Number of Countries: 001 Number of Patents: 002
Patent Family:

```
Patent No      Kind   Date     Applicat No     Kind   Date      Week
US 20020179965  A1  20021205  US 2001863448    A    20010524  200320  B
                              US 2002196126    A    20020717
US 6635531      B2  20031021  US 2001863448    A    20010524  200370
                              US 2002196126    A    20020717
```

Priority Applications (No Type Date): KR 200028366 A 20000525
Patent Details:

```
Patent No   Kind Lan Pg   Main IPC     Filing Notes
US 20020179965 A1    16 H01L-029/788  Div ex application US 2001863448
US 6635531    B2       H01L-021/336  Div ex application US 2001863448
                                     Div ex patent US 6501124
```

Abstract (Basic): US 20020179965 A1
Abstract (Basic):

NOVELTY - A **non-volatile semiconductor memory** device comprises:

(i) a **semiconductor substrate** (60) having a device active area and a device isolation area;

(ii) a **control gate** (62) that divides the device active area;

(iii) a **control gate insulating layer;**

(iv) a first **insulating layer;**

(v) a **drain region;**

(vi) a **source region** that is separated from the **control gate;**

(vii) a second **insulating layer;** and

(viii) a **floating gate** (69).

DETAILED DESCRIPTION - A **non-volatile semiconductor memory** device comprises:

(a) a **semiconductor substrate** having a device active area and a device isolation area;

(b) a **control gate** that divides the device active area into first and second regions;

(c) a **control gate insulating layer** between the substrate and the **control gate;**

(d) a first **insulating layer** covering a top surface and a side of the **control gate;**

(e) a **drain region** (67) in the first region of the substrate;

(f) a **source region** (72) that is separated from the **control gate;**

(g) a second **insulating layer** formed on a second **region** between the **source region** and the

control gate and formed on a portion of a surface of the first region adjacent the first **insulating layer** and over the **drain region**; and

(h) a **floating gate** covering the second and the first **insulating layer**.

INDEPENDENT CLAIMS are included for the following:

(a) a method of fabricating a **non-volatile semiconductor memory** device comprising forming a **control gate** on a portion of a memory cell area of a semiconductor area; providing a **control gate insulating layer** between the **control gate** and the substrate; forming a first **insulating layer** on an exposed surface of the **control gate**; forming a **drain region** in the first region; forming a third **insulating layer**; forming a **floating gate**; and forming a **source region**; and

(b) a method of preventing disturbance of a **non-volatile semiconductor memory** comprising providing a **non-volatile semiconductor memory** device; generating a first electric charge of a first parasitic **capacitance** from an applied **control gate** voltage and a **floating gate** voltage as a function of the first parasitic **capacitance** with respect to the difference between the **control gate** voltage and the **floating gate** voltage; generating a third electric charge of a third parasitic **capacitance** from a source voltage at the source junction and the induced **floating gate** voltage as a function of the third **capacitance** with respect to the difference between the source voltage and the **floating gate** voltage; generating a fourth electric charge of a fourth parasitic **capacitance**; generating a second electric charge of a second parasitic **capacitance**; selecting one of the **control gate** voltage and the drain voltage to reduce disturbances at wordline and bit line (74) where the **floating gate** voltage is determined by the **capacitance** of the first and the second **capacitors**, the **control gate** voltage, the drain voltage and the total parasitic **capacitance**; and programming the semiconductor memory by (Fowler-Nordhein) F-N tunneling or erasing by discharging electrons.

USE - As **non-volatile semiconductor memory** device.

ADVANTAGE - The invention prevents programming disturbance and enables programming operated by a byte unit by achieving a programming and an erasing of a memory device through a F-N tunneling using a coupling ratio between **floating** and **control gates** by forming a structure where the **control gate** is covered with the **floating gate**, a **drain region** is properly overlapped by coupling, and a **source region** is less overlapped. It has improved integration by reducing an area occupied by each of the memory cells. It consumes a low amount of current since the programming and the erasing can be achieved by F-N tunneling, thus reducing power consumption. It can be used with a single power source or low voltage operated products. It can be programmed at a low level since the threshold voltage for programming is low enough not to form a channel on reading and the threshold voltage for erasing has negative value, thus enabling the capability of use with a single power source and low voltage operated products.

DESCRIPTION OF DRAWING(S) - The figure shows a cross-sectional view of an electrically erasable and programmable ROM (**EEPROM**) device in semiconductor device.

Semiconductor substrate (60)

Control gate (62)
Poly-silicon layer (64)
Drain region (67)
Tunneling oxide **layer** (68)
Floating gate (69)
Source region (72)
Bit line (74)
pp; 16 DwgNo 2A/5

33/3,AB/2 (Item 2 from file: 350)
DIALOG(R)File 350:Derwent WPIX

014432923
WPI Acc No: 2002-253626/200230
Related WPI Acc No: 2001-396437
XRPX Acc No: N02-195734

Semiconductor memory device manufacturing method e.g. for **non-volatile memory**, involves forming **gate electrode** inside trench and implanting ions vertically inside trench and over substrate, to form corner dopant area

Patent Assignee: ADVANCED MICRO DEVICES INC (ADMI)
Inventor: LIU Y W
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 6303437	B1	20011016	US 9852058	A	19980330	200230	B
			US 2000632536	A	20000804		

Priority Applications (No Type Date): US 9852058 A 19980330; US 2000632536 A 20000804
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 6303437	B1		21	H01L-021/336	Div ex application US 9852058

Abstract (Basic): US 6303437 B1
Abstract (Basic):

NOVELTY - A trench (310) on a substrate (302) is etched vertically, to form a channel region (312) and **insulating layer** (314). A **gate electrode** is formed on the **insulating layer** in the trench. A **dielectric layer** (320) is formed on the **gate electrode**. Specific ions are implanted along vertical sides of trench and over substrate to form corner dopant area (324). **Source** and **drain regions** are formed in the junction of substrate, by ion doping.

USE - E.g. for manufacture of **non-volatile memory** like ROM, **EPROM**, **EEPROM**, flash **EEPROM** with trenched gate.

ADVANTAGE - Improves process control and manufacturability of devices, by maintaining planarity of **floating gate**. Reduces misalignment between **control gate** and **source-drain regions**, by reducing **capacitance coupling** due to formation corner doping area.

DESCRIPTION OF DRAWING(S) - The figure shows a cross-sectional view of **semiconductor substrate** under specific manufacturing process.

Substrate (302)
Trench (310)
Channel region (312)

Insulating layer (314)
Dielectric layer (320)
Corner dopant area (324)
pp; 21 DwgNo 3J/4

33/3,AB/3 (Item 3 from file: 350)
DIALOG(R)File 350:Derwent WPIX

013923278
WPI Acc No: 2001-407491/200143
XRPX Acc No: N01-301454

Non-volatile memory such as **EPROM, EEPROM** has integrated **dielectric film** formed on upper **floating gate**, with shape that does not rise perpendicular to **semiconductor substrate**

Patent Assignee: NEC CORP (NIDE); KANAMORI K (KANA-I)
Inventor: KANAMORI K
Number of Countries: 003 Number of Patents: 004
Patent Family:

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Patent No      Kind   Date     Applicat No    Kind   Date      Week
US 20010005029  A1  20010628  US 2000730312    A   20001205  200143  B
JP 2001185631   A   20010706  JP 99364871      A   19991222  200144
KR 2001062632   A   20010707  KR 200080380     A   20001222  200175
US 6339242      B2  20020115  US 2000730312    A   20001205  200208
```

Priority Applications (No Type Date): JP 99364871 A 19991222
Patent Details:

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Patent No  Kind Lan Pg   Main IPC    Filing Notes
US 20010005029 A1    19 H01L-029/788
JP 2001185631 A     14 H01L-021/8247
KR 2001062632 A        H01L-027/115
US 6339242    B2       H01L-029/72
```

Abstract (Basic): US 20010005029 A1
Abstract (Basic):

NOVELTY - Lower **floating gates** (FGs) (215) are formed on a **gate dielectric film** (202), in area between the **source** and **drain regions** (211,212) and in direction in which the **source** and **drain regions** extend. Upper FGs (216) are formed on the surfaces of the lower FGs, extending towards the region in which mounds (203) are formed. **Control gates** (CGs) (218) are formed on upper FGs through ONO film (217) formed in a shape not rising perpendicular to substrate (201).

DETAILED DESCRIPTION - **Source** and **drain regions** are formed below the **surface** of the **semiconductor substrate**, in parallel to each other. The mounds are formed on the surface of the **gate dielectric film** (202) provided on substrate and on both sides of lower **floating gates** extending in the direction along which the **source** and **drain regions** extend. The **interlayer dielectric films** (204) are formed on both sides of lower **floating gates** covering the mounds. An INDEPENDENT CLAIM is also included for fabrication method of **non-volatile memory**.

USE - **Non-volatile memory** such as **flash memory, EPROM, EEPROM.**

ADVANTAGE - The configuration of the memory increases **capacitance** between **control gate** and upper **floating gate**, and decreases the voltage that is applied to

the **control gate** to **control** the electrons of the **floating gate**.

DESCRIPTION OF DRAWING(S) - The figure shows the vertical section of **non-volatile memory** cut at position of transistor element.

Semiconductor substrate (201)
Dielectric films (202,204)
Mounds (203)
Source region (211)
Drain region (212)
Floating gates (215,216)
ONO film (217)
Control gate (218)
pp; 19 DwgNo 4a/7

33/3,AB/4 (Item 4 from file: 350)
DIALOG(R)File 350:Derwent WPIX

013912224
WPI Acc No: 2001-396437/200142
Related WPI Acc No: 2002-253626
XRPX Acc No: N01-291993

Trenched gate type **non-volatile semiconductor** device e.g. ROM for low power application, has corner dopings disposed such that their side surface is close to trench side wall and top surface is contiguous to substrate

Patent Assignee: ADVANCED MICRO DEVICES INC (ADMI)
Inventor: LIU Y W
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 6225659	B1	20010501	US 9852058	A	19980330	200142	B

Priority Applications (No Type Date): US 9852058 A 19980330
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 6225659	B1		15	H01L-029/76	

Abstract (Basic): US 6225659 B1
Abstract (Basic):

NOVELTY - A trench-to-**gate insulating layer** (214) is formed in a trench (212) formed between n-type **source region** (208) and **drain region** (210). An intergate **dielectric layer** (218) is formed on trenched **floating gate** (216) which is formed in trench and on layer (214). A **control gate electrode** (220) is formed on layer (218). P-type corner dopings (226) are disposed such that their side surface is close to trench side wall and top surface is contiguous to substrate (202).

DETAILED DESCRIPTION - The trench having substantially upright vertical side walls and bottom surface of selected depth below top **surface of semiconductor substrate,** is formed within p-type well junction **region** between n-type **source** and **drain regions** in the substrate. The **source** and **drain regions** are disposed close to the side wall of the trench and lower boundaries of **source** and **drain regions** are disposed at depths that are approximately less than the selected depth of bottom surface of trench. A channel region (211) is formed beneath the bottom surface of the trench. An intergate **dielectric layer** is formed on trenched **floating gate electrode** which is formed in trench and on trench-to-gate **insulating layer**, for electrically isolating the trenched **floating gate electrode**. A **control gate** is formed on the integrate **dielectric layer**. P-type corner dopings are formed within the well junction region in the substrate.

USE - E.g. read only memory (ROM), electrically erasable programmable read only memory (**EEPROM**), erasable programmable read only **memory** (**EPROM**) and **flash EEPROM** used for lower power applications.

ADVANTAGE - The trenched **floating gate** device has more planar topography resulting from reduced stacked **gate** height. Improves process **control** and manufacturability of devices. The corner dopings minimize the sensitivity to misalignments between **control gate**, **source** and **drain regions** by reducing the **capacitance coupling** between **control gate source** and **drain regions**. Improves isolation by reducing leakages through corners of trench in which the trenching **floating gate** is formed.

DESCRIPTION OF DRAWING(S) - The figure shows the cross-sectional view of dual gate device.

Substrate (202)
N-type **source region** (208)
Drain region (210)
Channel region (211)
Trench (212)
Insulating layer (214)
Floating gate (216)
Dielectric layer (218)
Gate electrode (220)
Corner dopings (226)
pp; 15 DwgNo 2B/4

33/3,AB/5 (Item 5 from file: 350)
DIALOG(R)File 350:Derwent WPIX

013242973
WPI Acc No: 2000-414855/200036
XRAM Acc No: C00-125908
XRPX Acc No: N00-309994

Semiconductor device gate electrode is formed on **gate insulating film** deposited by CVD between **source/ drain regions** formed on **semiconductor substrate**

Patent Assignee: TOSHIBA KK (TOKE); TOSHIBA CORP (TOKE)
Inventor: AKAHORI H; KATSUI S; MIKATA Y
Number of Countries: 029 Number of Patents: 005
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
EP 1017089	A2	20000705	EP 99124849	A	19991215	200036	B
JP 2000183346	A	20000630	JP 98375423	A	19981215	200037	
KR 2000048156	A	20000725	KR 9957944	A	19991215	200116	
US 6713824	B1	20040330	US 99459913	A	19991214	200423	
TW 560067	A	20031101	TW 99121910	A	19991214	200425	

Priority Applications (No Type Date): JP 98375423 A 19981215
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 1017089	A2	E	12	H01L-021/28	
JP 2000183346	A		7	H01L-029/78	
KR 2000048156	A			H01L-029/78	
US 6713824	B1			H01L-029/76	
TW 560067	A			H01L-029/78	

Designated States (Regional): AL AT BE CH CY DE DK ES FI FR GB GR IE IT LI LT LU LV MC MK NL PT RO SE SI (EP 1017089)

Abstract (Basic): EP 1017089 A2

Abstract (Basic):

NOVELTY - (**Floating**) **gate electrode** (123a) having film stress at most 200 MPa in absolute value terms is formed on a **gate insulating film** (122) deposited by a CVD process at 640 degrees C or more, preferably 650 degrees C, between **source/drain regions** (124) formed on a **semiconductor substrate** (121). The **gate electrode** preferably comprises a polysilicon film which is formed while rotating the substrate at 3000 rpm or more.

DETAILED DESCRIPTION - INDEPENDENT CLAIMS are given for:

(a) a semiconductor device prepared as above, where the **gate electrode** is in contact with the **gate electrode** which is formed of a polysilicon film, or comprises at least one metal silicide film and a high melting point metal film, the high melting point film being formed on the metal silicide film; and

(b) a **non-volatile semiconductor** device having a **floating gate** formed on a **gate insulating film**.

USE - Production of semiconductor device having MOS transistor formed in it, particularly a non-volatile storage device such as **EEPROM.**

ADVANTAGE - Improved **gate electrode** reliability by increasing the a total charge amount Qbd by suppressing film stress of the **gate electrode** to a low value.

DESCRIPTION OF DRAWING(S) - The drawing shows a cross-sectional view of a **semiconductor substrate** having a MOS **capacitor** according to the invention.

Silicon **semiconductor substrate** (121)
Gate insulating film (122)
Polysilicon film (123)
Gate electrode (123a)
Source/drain regions (124)
pp; 12 DwgNo 2/10

33/3,AB/6 (Item 6 from file: 350)
DIALOG(R)File 350:Derwent WPIX

012892879
WPI Acc No: 2000-064714/200006
XRAM Acc No: C00-018221
XRPX Acc No: N00-050770

Manufacture of **non-volatile semiconductor memory** devices such as **EEPROM** devices and flash **EEPROM** devices

Patent Assignee: EM MICROELECTRONIC MARIN SA (EMMI-N); LOJEK B (LOJE-I)
Inventor: BOHUMIL L; LOJEK B
Number of Countries: 028 Number of Patents: 005
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week

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EP 967654       A1   19991229  EP 98111779     A   19980626  200006  B
JP 2000031307   A    20000128  JP 99181355     A   19990628  200017
TW 434551       A    20010516  TW 99110494     A   19990622  200170
US 6346443      B1   20020212  US 99337513     A   19990622  200219
US 20020033517  A1   20020321  US 99337513     A   19990622  200224
                               US 2001950683   A   20010913

Priority Applications (No Type Date): EP 98111779 A 19980626
Patent Details:
Patent No  Kind Lan Pg   Main IPC    Filing Notes
EP 967654     A1 E  15 H01L-027/115
   Designated States (Regional): AL AT BE CH CY DE DK ES FI FR GB GR IE IT
   LI LT LU LV MC MK NL PT RO SE SI
JP 2000031307 A      8 H01L-021/8247
TW 434551     A        G11C-016/00
US 6346443    B1       H01L-021/336
US 20020033517 A1       H01L-027/10   Div ex application US 99337513
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Abstract (Basic): EP 967654 A1

Abstract (Basic):

NOVELTY - The **non-volatile memory** device is formed of an array of memory cells (10), each memory cell comprising a gate structure formed of a first **dielectric layer**, a **floating gate** (124), a second **dielectric layer** and a **control gate** (128) formed in a well. The **control gate** overlaps the **floating gate** along the sidewalls of the well.

DETAILED DESCRIPTION - Forming a **non-volatile semiconductor memory** device formed of an array of memory cells (10) organized into rows (20) and columns (22) within a **semiconductor substrate** (100) comprises:

(a) performing a blanket implant in the **semiconductor substrate** resulting in the formation of a uniformly doped region (150);

(b) forming insulating trenches (200) in the substrate in a direction parallel to the columns (22);

(c) forming wells (50) in the substrate between the insulating trenches to define alternated source (152) and **drain** (154) **regions** along the columns (22), each well has a bottom surface (52) and facing sidewalls (54,56) being respectively adjacent to **source** and **drain regions** and to insulating trenches;

(d) forming a first **dielectric layer** (122) over the substrate surface and the wells;

(e) forming first conductive **layer** (124) over first **dielectric layer** (122);

(f) removing portions of the first conductive layer to define strips overlying the wells in a direction parallel to the column;

(g) forming a second **dielectric layer** (126) over the first conductive layer (124);

(h) forming a second conductive layer (128) over the second **dielectric layer** (126); and

(i) removing portions of first and second conductive layers (124,128) and second **dielectric layer** (126) to define gate structures (120) overlying wells along rows (20).

An INDEPENDENT CLAIM is also included for a **non-volatile memory** device formed as above.

USE - **Non-volatile semiconductor memory** devices such as **EEPROM** devices and flash **EEPROM** devices.

ADVANTAGE - The surface area of the memory device is reduced, due to the fact that each memory cell is formed in a well, the whole surface of the memory device is reduced and reliability of the memory cells is increased. Manufacturing costs are reduced. The **capacitive coupling** between the **floating gate** and the **control gate** of the memory cells is improved. The performances of the memory device are improved.

DESCRIPTION OF DRAWING(S) - The drawing shows an **EEPROM** device of the invention.

EEPROM cells (10)
Rows of **EEPROM** cells (20)
Columns (22)
Floating gate (124)
Control gate (128)
Source (152)
Drain (154)
Insulating trenches (200)
pp; 15 DwgNo 3/8

33/3,AB/7 (Item 7 from file: 350)
DIALOG(R)File 350:Derwent WPIX

010918226
WPI Acc No: 1996-415177/199642
XRPX Acc No: N96-349488

Non-volatile ferroelectric **memory** - has **gate electrode** on **gate** ferroelectric film on gate yttrium oxide film formed on **semiconductor substrate** and **source-drain region** either sides of **gate electrode**

Patent Assignee: SAMSUNG ELECTRONICS CO LTD (SMSU)
Inventor: MOON J
Number of Countries: 006 Number of Patents: 008
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
GB 2299208	A	19960925	GB 966024	A	19960322	199642	B
DE 19610907	A1	19960926	DE 1010907	A	19960320	199644	
JP 8264669	A	19961011	JP 9647729	A	19960305	199651	
TW 291599	A	19961121	TW 96102575	A	19960302	199712	
US 5621681	A	19970415	US 96620209	A	19960322	199721	
US 5744374	A	19980428	US 96620209	A	19960322	199824	
			US 96751389	A	19961118		
GB 2299208	B	19981230	GB 966024	A	19960322	199903	
KR 141160	B1	19980601	KR 956108	A	19950322	200015	

Priority Applications (No Type Date): KR 956108 A 19950322
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
GB 2299208	A		24	H01L-029/78	
DE 19610907	A1		10	H01L-027/105	
JP 8264669	A		7	H01L-021/8247	
US 5621681	A		9	H01L-027/108	
US 5744374	A		9	H01L-021/70	Div ex application US 96620209 Div ex patent US 5621681
KR 141160	B1			H01L-027/085	
TW 291599	A			H01L-027/01	
GB 2299208	B			H01L-029/78	

Abstract (Basic): GB 2299208 A

The memory includes a MISFET structure and uses a yttrium oxide film (11a) as a buffer film. The device comprises a P-type silicon

substrate (1), a field oxide film (2) formed in a device isolation region of the substrate, a gate yttrium oxide film, a gate ferroelectric film, a **gate** TiN **electrode** (13a) and an N-type **source-drain region** (3) on both sides of the **gate electrode** (13a).

An LDD structure is provided with a spacer SiON film over the gate structure and an impurity **region** above the **source-drain region**. The **insulating film** which is well matched with silicon in terms of lattice constant and thermal expansion coefficient.

USE/ADVANTAGE - For **EEPROM.** Films have enhanced polarisation characteristics. Has excellent current-voltage and **capacitance** -voltage characteristics when yttrium oxide **film** is used as **insulating film**.

Dwg.2/5

Abstract (Equivalent): US 5621681 A

A ferroelectric memory device comprising:

a **semiconductor substrate** of a first conductive type;

a yttrium oxide (Y2O3) gate film formed over the **semiconductor substrate;**

a ferroelectric gate film formed over the yttrium oxide film;

a **gate electrode** formed over the ferroelectric film; and

a **source/drain region** of a second conductive type different from the first conductive type, formed in said **semiconductor substrate** along sides of the **gate electrode.**

Dwg.3/5e

33/3,AB/8 (Item 8 from file: 350)
DIALOG(R)File 350:Derwent WPIX

010795686
WPI Acc No: 1996-292639/199630
XRPX Acc No: N96-245933

Semiconductor memory write-in unit - has impurity-diffusion layer to determine condition of slope angle larger than stored write-in information when signal is applied to **control gate**

Patent Assignee: NEC CORP (NIDE)
Inventor: HARA H
Number of Countries: 002 Number of Patents: 002
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
JP 8124391	A	19960517	JP 94255034	A	19941020	199630	B
US 5544099	A	19960806	US 95543818	A	19951016	199637	

Priority Applications (No Type Date): JP 94255034 A 19941020
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
JP 8124391	A		7	G11C-016/06	
US 5544099	A		16	G11C-016/04	

Abstract (Basic): JP 8124391 A

The unit has a **floating gate** formed through a first **insulating film** on a **semiconductor substrate** having a source area with an impurity-diffusion layer and a drain area corresp. to the semiconductor memory. The unit has a **control gate** formed through a second **gate insulating** layer on the **floating gate.**

The unit applies a signal to the **control gate** and stores a write-in information smaller than the angle of a slope. The condition of the slope angle of the straight line produces a transition to a low voltage state from the signal of a high voltage state by a time constant. The condition is decided by the **capacitance** and the resistance of the impurity-diffusion layer.

USE/ADVANTAGE - For electrically erasable programmable read-only memory. Regulates limit-value variation of **control gate** since it prevents flow of forward current in drain source; improves repetition tolerance of write-in data.

Dwg.1/9

Abstract (Equivalent): US 5544099 A

A method of writing data into a memory cell, comprising steps of:

a) preparing a **semiconductor non-volatile memory** device including a plurality of **floating gate** type field effect transistors serving as addressable memory cells and grouped into a plurality of sectors, each of said plurality of **floating gate** type field effect transistors having **source** and **drain regions** spaced from each other, a **floating gate electrode** associated with said **source** and **drain regions** and electrically isolated from said **source** and **drain regions** and a **control gate electrode** associated with said **source** and **drain regions** and electrically isolated from said **floating gate electrode** and said **source** and **drain regions,**

a plurality of word lines shared between said plurality of sectors and selectively connected to **control gate electrodes** of said plurality of **floating gate** type field effect transistors, and

an addressing system having a row addressing subsystem for selectively supplying a write-in pulse signal to said plurality of word lines;

b) increasing said write-in pulse signal on a selected one of said plurality of word lines for writing data into at least one **floating gate** type field effect transistor of a selected one of said plurality of sectors; and

c) decaying said write-in pulse along a waveform having a first gradient smaller than a second gradient of a waveform of a pulse signal applied to one of said **source** and **drain regions** forming a part of the **floating gate** type field effect transistor incorporated in a non-selected one of said sectors and coupled to said selected one of said plurality of word lines.

Dwg.7,8/10

33/3,AB/9 (Item 9 from file: 350)
DIALOG(R)File 350:Derwent WPIX

010724304
WPI Acc No: 1996-221259/199622
XRAM Acc No: C96-070148
XRPX Acc No: N96-185763

Method of mfg. a **non-volatile memory** used for **EPROM**, mask ROM and DRAM - by forming **floating gate** on **insulating film** of substrate, implanting impurity ions on one side of **gate**, forming second **insulating film** followed by conductive film, implanting impurity ions into conductive film and

patterning
Patent Assignee: SHARP KK (SHAF)
Inventor: YAMAUCHI Y
Number of Countries: 002 Number of Patents: 002
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 5510284	A	19960423	US 94247889	A	19940523	199622	B
			US 95508132	A	19950727		
JP 7115143	A	19950502	JP 9473603	A	19940412	199622	

Priority Applications (No Type Date): JP 9473603 A 19940412; JP 93212958 A 19930827
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 5510284	A		10	H01L-021/8247	Cont of application US 94247889
JP 7115143	A		7	H01L-021/8247	

Abstract (Basic): US 5510284 A

A method of mfg. a **non-volatile memory** comprises: forming a **floating gate** (3) on an **insulator** (2) on a **semiconductor substrate** (1); implanting impurity ions adjacent to one side of the gate while masking the other side; forming a second **insulating film** (7) followed by a conductive film, which is higher on a gate sidewall than its horizontally extending portion; implanting impurity ions into the substrate via the conductive film to form an offset region (13) between the gate and a **source/drain region**; and patterning the conductive film to form a **control gate** (15).

USE - As **non-volatile memories** on p- or n-Si such as EPROMs, flash EEPROMs, mask ROMs and DRAMs.

ADVANTAGE - Substrate damage is prevented as is filed inversion voltage decrease caused by filed oxide thinning; memory **capacity** is thus enlarged.

Dwg.4/15

33/3,AB/10 (Item 10 from file: 350)
DIALOG(R)File 350:Derwent WPIX

010647709
WPI Acc No: 1996-144663/199615
XRAM Acc No: C96-045357
XRPX Acc No: N96-121431

Non-volatile semiconductor memory with **floating gate** type memory cell e.g. **EEPROM** - has **control gate electrode** contacting under surface of **floating gate electrode** through **interlayer insulating film**

Patent Assignee: NIPPON STEEL CORP (YAWA)
Inventor: SATO Y
Number of Countries: 002 Number of Patents: 003
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
JP 8031959	A	19960202	JP 94180697	A	19940708	199615	B
US 5594688	A	19970114	US 95499379	A	19950707	199709	
US 5686333	A	19971111	US 95499379	A	19950707	199751	
			US 96736059	A	19961022		

Priority Applications (No Type Date): JP 94180697 A 19940708

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
JP 8031959	A		10	H01L-021/8247	
US 5594688	A		13	H01L-029/788	
US 5686333	A		16	H01L-021/8247	Div ex application US 95499379 Div ex patent US 5594688

Abstract (Basic): JP 8031959 A

The memory has a P type silicon **semiconductor substrate** (11) on which an element isolation film (21) is formed. A **floating gate electrode** (23) is formed on the element isolation film, with a clearance domain between them. A source diffusion layer (13) and a drain diffusion layer (12) are formed on the substrate.

The **floating gate electrode** touches the channel domain formed between the source diffusion layer and the drain diffusion **layer** through a **tunnel** oxide **film**. An **interlayer insulating film** (16) is formed above the **floating gate electrode**. A **control gate electrode** (22) contacts the **floating gate electrode** through the **interlayer insulating film**.

ADVANTAGE - Increases **capacitive coupling** ratio without enlarging area of memory cell. Improves yield and through-put. Reduces number of processes during mfg of memory cell.

Dwg.1/10

Abstract (Equivalent): US 5686333 A

A method of producing a **nonvolatile semiconductor memory** device comprising the steps of: selectively forming element isolation **insulating films** in a **surface** of a **semiconductor substrate**; forming a first polycrystalline silicon film over the **surface** of the **semiconductor substrate**; selectively etching the first polycrystalline silicon film to thereby partially expose the element isolation **insulating films**;

partially etching each of the element isolation **insulating films** using the first polycrystalline silicon film as a mask to form a gap between a portion of each of the element isolation **insulating films** underlying the first polycrystalline silicon film and the first polycrystalline silicon film; and successively forming an **interlayer insulating film** and a second polycrystalline silicon film over an entire **surface** of the **semiconductor substrate** to form the **nonvolatile memory** device.

Dwg.1A/8

US 5594688 A

A **nonvolatile semiconductor memory** device comprising:

a **semiconductor substrate** of a first conductivity type;

at least a pair of element isolation **insulating films**;

a pair of spaced **source**/drawn **regions** of a second conductivity type different from the first conductivity type and formed in a **surface** of the **semiconductor substrate**;

a **floating gate electrode** formed above a channel region disposed between the pair of **source/drain regions** in the **surface** of the **semiconductor substrate** in an insulated relationship with the channel region, where the **floating gate electrode** overlaps each of the element isolation **insulating films** and a gap is formed

between an underside of the **floating gate electrode** and each of the element isolation **insulating films** at each of portions of it where the **floating gate electrode** overlaps the pair of element isolation **insulating films**, respectively; and

a **control gate electrode** formed above the **floating gate electrode** in an **insulated** relationship with the **floating gate electrode**, where a part of the **control gate electrode** extends beyond a side of the **floating gate electrode** to an underside of the **floating gate electrode** facing each of the gaps.

Dwg.1/7

33/3,AB/11 (Item 11 from file: 350)
DIALOG(R)File 350:Derwent WPIX

010278650
WPI Acc No: 1995-179906/199524
XRAM Acc No: C95-083389
XRPX Acc No: N95-141197

Non-volatile memory, esp. **EPROM** or **EEPROM** - has high programming speed, integration density and coupling degree

Patent Assignee: GOLDSTAR ELECTRON CO LTD (GLDS); LG SEMICON CO LTD (GLDS)
Inventor: HWANG H S
Number of Countries: 002 Number of Patents: 004
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
DE 4335834	A1	19950511	DE 4335834	A	19931020	199524	B
US 5459091	A	19951017	US 93135261	A	19931012	199547	N
US 5793080	A	19980811	US 93135261	A	19931012	199839	N
			US 95478472	A	19950607		
			US 96718224	A	19960920		
DE 4335834	C2	20030528	DE 4335834	A	19931020	200337	

Priority Applications (No Type Date): DE 4335834 A 19931020; US 93135261 A 19931012; US 96718224 A 19960920

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
DE 4335834	A1		11	H01L-027/115	
US 5459091	A			H01L-021/8247	
US 5793080	A			H01L-029/788	Div ex application US 93135261 Cont of application US 95478472 Div ex patent US 5459091
DE 4335834	C2			H01L-027/115	

Abstract (Basic): DE 4335834 A

Mfr. of a **non-volatile memory** involves (a) CVD of an oxide film over a **semiconductor substrate** of first conductivity type; (b) photoetching of the oxide film to leave a portion on the substrate; (c) formation of a gate oxide film on the exposed portion of the substrate; (d) successive application of a first polysilicon **film**, an **insulating film** and a second polysilicon film over the entire structure; (e) back-etching of the polysilicon and **insulating film** to form a gate consisting of (i) a potential-free gate on a CVD oxide film sidewall and having one region, lying flat over the gate oxide film, and another integral

region, extending at right angles from the end of the first region, (ii) an intermediate isolating **film** providing high **capacitance** and (iii) a **control gate** extending over the other end section of the flat region of the potential-free gate and at right angles to the flat region; (f) implantation of second conductivity type dopant into the substrate to produce a high density **drain region** with a flat junction; (g) elimination of the CVD oxide film, deposition of an oxide film over the entire structure and anisotropic etching of the oxide film to form spacers on both sides of the gate; and (h) implantation of second conductivity type dopant into the substrate to produce high density **source** and **drain regions** with deep junctions. A **non-volatile memory** is also claimed.

USE - As an **EPROM** or **EEPROM.**

ADVANTAGE - The memory has high programming speed at low voltage and a high integration density, together with high coupling degree, maximised **gate** current and a **control gate** and potential-free gate with sizes in the lower submicron range.

(Dwg.1h/6

33/3,AB/12 (Item 12 from file: 350)
DIALOG(R)File 350:Derwent WPIX

009442848
WPI Acc No: 1993-136365/199317
XRPX Acc No: N93-103991

Non-volatile semiconductor memory e.g **flash eeprom** - has **control gate** with low impurity concentration region reducing **capacitance** between **control** and **floating gates**

Patent Assignee: TOSHIBA KK (TOKE)
Inventor: MIYAMOTO J; NARUKE K; YOSHIKAWA K
Number of Countries: 006 Number of Patents: 009
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
EP 539184	A2	19930428	EP 92309628	A	19921021	199317	B
JP 5121755	A	19930518	JP 91303830	A	19911024	199324	
US 5365098	A	19941115	US 92963622	A	19921020	199445	
EP 539184	A3	19930811	EP 92309628	A	19921021	199507	
EP 539184	B1	19970409	EP 92309628	A	19921021	199719	
DE 69218878	E	19970515	DE 618878	A	19921021	199725	
			EP 92309628	A	19921021		
KR 124500	B1	19971211	KR 9219520	A	19921023	199951	
KR 99008586	A	19990205	KR 9730617	A	19970702	200015	
KR 271341	B1	20001101	KR 9219520	A	19921023	200139	
			KR 9730617	A	19970702		

Priority Applications (No Type Date): JP 91303830 A 19911024
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 539184	A2	E	15	H01L-029/788	
Designated States (Regional): DE FR GB					
JP 5121755	A			H01L-029/788	
US 5365098	A		12	H01L-029/68	
EP 539184	A3			H01L-029/788	
EP 539184	B1	E	15	H01L-029/788	
Designated States (Regional): DE FR GB					
DE 69218878	E			H01L-029/788	Based on patent EP 539184

KR 124500	B1	H01L-029/68	
KR 99008586	A	H01L-027/10	
KR 271341	B1	H01L-000/00	Div ex application KR 9219520

Abstract (Basic): EP 539184 A

The device has a **floating gate** (43) is formed via a first **gate insulating film** (44) over the channel **region** between **source** and **drain regions** (41,42) formed in a **semiconductor substrate** (40). A **control gate** (45) is formed over the **floating gate** (43). A low impurity concentration region (45a) is formed on the side of the **control gate** which faces the **floating gate.**

When erasing a depletion layer (45b) is produced in the low impurity concentration region and further saturates the erase characteristic for the erasure time by decreasing the **capacitance** between the **control gate** and the **floating gate** (43).

ADVANTAGE - Reduces randomness of erasure characteristic due to randomness of structural parameter.

Dwg.4/12

Abstract (Equivalent): EP 539184 B

A **non-volatile semiconductor memory** comprising

a **semiconductor substrate** (40) of first conductivity type having a main surface, a **source region** (41) of second conductivity type formed on the main surface, a **drain region** (42) of second conductivity type formed on the main surface apart from the **source region** (41), a channel **region** between the **source region** (41) and the **drain region** (42), a **floating gate electrode** (43) formed over the channel region and electrically isolated from the substrate (40), the **source region** (41) and the **drain region** (42); and

a **control gate electrode** (45) formed over the **floating gate electrode** (43) and isolated from the **floating gate electrode** (43), the **control gate electrode** (45) having a **floating gate electrode** side facing the **floating gate electrode** (43) and an upper side remote therefrom, characterised in that

the **control gate electrode** (45) has a graded impurity concentration such that the impurity concentration is lower on the **floating gate electrode** side of the **control gate electrode**, forming a low impurity concentration region (45a), and is higher on the upper side of the **control gate electrode**.

Dwg.2/12

Abstract (Equivalent): US 5365098 A

A **floating gate** is formed via a first **gate insulating film** over the channel **region** between **source** and **drain regions** which are formed in a **semiconductor substrate.** A **control gate** is formed via a second **gate insulating film** over the **floating gate.** A low impurity concentration semiconductor region is formed on the side of the **control gate** which faces the **floating gate.**

When erasing, a depletion layer is produced in this low impurity concentration region and further saturates the erase characteristic for the erasure time by decreasing the **capacitance** between the **control gate** and the **floating gate.**

ADVANTAGE - Reduces randomness of erasure characteristic due to randomness of structural parameters.
Dwg.4/12

33/3,AB/13 (Item 13 from file: 350)
DIALOG(R)File 350:Derwent WPIX

009273445
WPI Acc No: 1992-400856/199249
XRPX Acc No: N92-305667
Flash-**EEPROM** or **EEPROM non-volatile memory**
cell - comprises transistor with source and drain connected using
capacitive data storage technique
Patent Assignee: GEMPLUS (GEMP-N); GEMPLUS CARD INT SA (GEMP-N)
Inventor: KOWALSKI J
Number of Countries: 008 Number of Patents: 008
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
EP 516516	A1	19921202	EP 92401408	A	19920522	199249	B
JP 5206478	A	19930813	JP 92164152	A	19920529	199337	
FR 2690008	A1	19931015	FR 916466	A	19910529	199349	
US 5552621	A	19960903	US 92888639	A	19920527	199641	
			US 94331871	A	19941101		
US 5721440	A	19980224	US 92888639	A	19920527	199815	
			US 94331871	A	19941101		
			US 96629550	A	19960409		
EP 516516	B1	19981111	EP 92401408	A	19920522	199849	
DE 69227542	E	19981217	DE 627542	A	19920522	199905	
			EP 92401408	A	19920522		
ES 2127210	T3	19990416	EP 92401408	A	19920522	199922	

Priority Applications (No Type Date): FR 916466 A 19910529
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 516516	A1	F	12	H01L-029/94	
Designated States (Regional): DE ES GB IT NL					
US 5552621	A		10	H01L-029/788	Cont of application US 92888639
US 5721440	A		10	H01L-029/788	Cont of application US 92888639
					Cont of application US 94331871
					Cont of patent US 5552621
EP 516516	B1	F		H01L-029/94	
Designated States (Regional): DE ES GB IT NL					
DE 69227542	E			H01L-029/94	Based on patent EP 516516
ES 2127210	T3			H01L-029/94	Based on patent EP 516516
JP 5206478	A			H01L-029/788	
FR 2690008	A1			H01L-027/115	

Abstract (Basic): EP 516516 A

The memory cell of an integrated circuit memory formed on a **semiconductor substrate** comprises a control grid, insulated from a floating grid which is itself insulated from the **semiconductor substrate**. This insulation comprises a window of oxide tunnel.

The cell comprises only one diffused region in the substrate with the grid overlying this part. This region is doped with impurities of opposite type to those in the substrate.

ADVANTAGE - Cell provides **capacitive** type **EEPROM** or FLASH-**EPROM** providing **non-volatile memory**.

y
Dwg.3/6
Abstract (Equivalent): US 5721440 A

The memory cell of an integrated circuit memory formed on a **semiconductor substrate** comprises a control grid, insulated from a floating grid which is itself insulated from the **semiconductor substrate**. This insulation comprises a window of oxide tunnel.

The cell comprises only one diffused region in the substrate with the grid overlying this part. This region is doped with impurities of opposite type to those in the substrate.

ADVANTAGE - Cell provides **capacitive** type **EEPROM** or FLASH-**EPROM** providing **non-volatile memory**.

y
1a,1b/5b
US 5552621 A

A memory cell for an integrated circuit memory, the cell having components mounted on a **semiconductor substrate** and further comprising:

a **control gate**;

a **floating gate**, **controlled** by the **control gate** and insulated from the **control gate**;

an **insulation layer** for **insulating** the **floating gate** from the substrate and including at least one tunnel window made of a tunnel oxide;

a transistor having a channel **region**, as well as **drain** and **source regions** diffused in the substrate and located adjacent the channel region;

and a conductor overlying and forming a permanent connection between the **drain** and **source regions**, the conductor extending in spaced overlying relation to the substrate and the **floating gate**.

Dwg.1a/5

33/3,AB/14 (Item 1 from file: 347)
DIALOG(R)File 347:JAPIO
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03692269
SEMICONDUCTOR INTEGRATED CIRCUIT

PUB. NO.: 04-057369 [JP 4057369 A]
PUBLISHED: February 25, 1992 (19920225)
INVENTOR(s): MATSUKAWA HISAHIRO
MIYAMOTO JUNICHI
APPLICANT(s): TOSHIBA CORP [000307] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 02-166913 [JP 90166913]
FILED: June 27, 1990 (19900627)
JOURNAL: Section: E, Section No. 1215, Vol. 16, No. 259, Pg. 32, June 11, 1992 (19920611)

ABSTRACT

PURPOSE: To make the high speed reading-out feasible for acturizing the high speed **EPROM**, high speed **EEPROM**, etc., by a method wherein the channel current of a memory cell transistor is amplified by a vertical type bipolar transistor.

CONSTITUTION: A **floating gate** 17 is arranged between a drain 14

and a source 13 provided on the surface of the first conductivity type **semiconductor substrate** 12 through the intermediary of a **gate insulating film** 16. Next, a laminated gate type **non-volatile memory** cell transistor whereon a **control gate** 19 is laminated on the **floating gate** 17 through the intermediary of an **interlayer insulating film** 18 as well as a vertical bipolar transistor using the **semiconductor substrate** 12 as a collector **region** while the **drain** 14 of the memory cell transistor as a base region on whose surface the first conductivity type emitter 20 is formed are provided. Through these procedures, the channel current of the **non-volatile memory** cell transistor can be amplified by the vertical bipolar transistor so that the bit line, etc., connected to the emitter 20 may be driven, thereby enabling the current driving **capacity** to be increased for making high speed readout feasible.

35/3,AB/1   (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX

016156119
WPI Acc No: 2004-314006/200429
XRPX Acc No: N04-250029

Nonvolatile semiconductor memory device e.g. asymmetrical contactless transistor **flash memory,** has main-bit lines connected to related sub-bit lines and two adjacent main-bit lines located on different **dielectric layers**

Patent Assignee: SHARP KK (SHAF)
Inventor: SUGITA Y; YAMAUCHI Y
Number of Countries: 002 Number of Patents: 002
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 20040051133	A1	20040318	US 2003657195	A	20030909	200429	B
JP 2004111478	A	20040408	JP 2002268937	A	20020913	200429	

Priority Applications (No Type Date): JP 2002268937 A 20020913
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 20040051133	A1		26	H01L-021/336	
JP 2004111478	A		18	H01L-021/8247	

Abstract (Basic): US 20040051133 A1
Abstract (Basic):

NOVELTY - The device has memory cells formed on a **semiconductor substrate** (1), each cell having an **insulating film** formed on the substrate surface between **source** and **drain regions**. Each main bit-line (12, 22) is formed on **dielectric layers** and is connected to a related sub-bit line via conductive unit penetrating through the **dielectric layer** under the main-bit line. Two adjacent main-bit lines are located on different **dielectric layers**.

DETAILED DESCRIPTION - An INDEPENDENT CLAIM is also included for a process for producing a **nonvolatile semiconductor memory** device.

USE - Used for storing data.

ADVANTAGE - Two adjacent main-bit lines are located on different **dielectric layers** such that the distance is long enough so that there is small **capacity** between the adjacent main-bit lines, thereby not affecting the non-selected main-bit line at the writing operation and hence preventing error-writing. The device maintains the writing rate.

DESCRIPTION OF DRAWING(S) - The drawing shows a cross section taken along a wordline of an asymmetrical contactless transistor **flash memory**.

Semiconductor substrate (1)
Source region (2)
Drain region (3)
Main-bit lines (12, 22)
Control gate (16)
pp; 26 DwgNo 1/17

38/3,AB/1 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX

016251774
WPI Acc No: 2004-409668/200438
XRAM Acc No: C04-153729
XRPX Acc No: N04-325279

Non-volatile memory for programming and reading data, has charge storage elements across **semiconductor substrate**, **control gate** lines across the storage elements, and decoder and voltage supply connected to the **control gate** lines

Patent Assignee: SANDISK CORP (SAND-N)
Inventor: HARARI E
Number of Countries: 106 Number of Patents: 002
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 20040079988	A1	20040429	US 2002282747	A	20021028	200438	B
WO 200440583	A1	20040513	WO 2003US32383	A	20031009	200439	

Priority Applications (No Type Date): US 2002282747 A 20021028
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 20040079988	A1		22	H01L-029/788	
WO 200440583	A1	E		G11C-016/04	

Designated States (National): AE AG AL AM AT AU AZ BA BB BG BR BY BZ CA CH CN CO CR CU CZ DE DK DM DZ EC EE EG ES FI GB GD GE GH GM HR HU ID IL IN IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MA MD MG MK MN MW MX MZ NI NO NZ OM PG PH PL PT RO RU SC SD SE SG SK SL SY TJ TM TN TR TT TZ UA UG UZ VC VN YU ZA ZM ZW

Designated States (Regional): AT BE BG CH CY CZ DE DK EA EE ES FI FR GB GH GM GR HU IE IT KE LS LU MC MW MZ NL OA PT RO SD SE SI SK SL SZ TR TZ UG ZM ZW

Abstract (Basic): US 20040079988 A1
Abstract (Basic):

NOVELTY - **Non-volatile memory** includes an array of charge storage elements across a **semiconductor substrate** ; **control gate** lines (81-84) extending across the array such that opposing sidewalls of individual charge storage elements are **capacitively coupled** with the **control gate** lines; and a decoder and voltage supply connected to the **control gate** lines to couple **controlled** voltages to the charge storage elements during programming and reading data.

DETAILED DESCRIPTION - INDEPENDENT CLAIMS are also included for:

(a) altering or determining charge states storage elements by applying first voltage levels to **control gates** that are both coupled with the storage elements to cause the charge states to be either altered or determined; simultaneously applying a second voltage level to a third **control gate** that is coupled with a first group of non-designated storage elements that are also coupled with one of the first or second **control gates** to combine to cause the charge states of the first group of non-designated storage elements to be neither altered nor determined; and simultaneously applying third voltage levels to additional **control gates** to which other non-designated storage elements are coupled to cause the charge states of the other non-designated storage elements to be neither altered nor determined;

(b) coupling voltages to storage elements for simultaneously programming or reading their charge storage states by applying different voltages to **control gates;**

(c) a **non-volatile memory** system comprising a memory cell array, and voltage supply circuit connected to the **control gate** lines that simultaneously provides two different voltage **control gate** lines;

(d) production of memory cell array on a **semiconductor substrate** by forming a rectangular array of columns and rows of **floating gates** across a surface area of the substrate with a first **layer** of **dielectric** between them; providing isolation of the **floating gates** across the substrate between columns; and forming **control gates** extending across the substrate area perpendicular to the columns between rows of the **floating gates**.

USE - For programming and reading data.

ADVANTAGE - By coupling the individual **floating gates** to the **control gates,** the height of the **floating gates** is increased and the total coupling area of the **floating gate** with the **control gates** is increased independent of the coupling area between the **floating gate** and the substrate. This allows the **control gate** voltages to be reduced but still results in increasing the voltage coupled to the **floating gates**.

DESCRIPTION OF DRAWING(S) - The figure shows a cross-sectional view of the NAND array.

Source and **drain region** (57,62,67,72,105,106)
Control gate lines (81-84)
Dielectric layer (103)
pp; 22 DwgNo 4/16

38/3,AB/2 (Item 2 from file: 350)
DIALOG(R)File 350:Derwent WPIX

016135380
WPI Acc No: 2004-293256/200427
XRAM Acc No: C04-112213
XRPX Acc No: N04-232819

Non-volatile memory array comprises H-shaped **source/drain regions** defined by field isolation regions and word lines, and each **source/drain region** serving as **source/drain** for four different **non-volatile memory** transistors

Patent Assignee: TOWER SEMICONDUCTOR LTD (TOWE-N)
Inventor: KIM J
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 20040041199	A1	20040304	US 2002233310	A	20020828	200427	B

Priority Applications (No Type Date): US 2002233310 A 20020828
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 20040041199	A1		23	H01L-029/788	

Abstract (Basic): US 20040041199 A1
Abstract (Basic):

NOVELTY - A **non-volatile memory** array comprises field isolation regions in a **semiconductor substrate;** word lines extending over the substrate along a first axis, where the word lines form **control gates** of the 2-bit **non-volatile memory** transistors; and H-shaped **source/drain regions** defined by the field isolation regions and the word lines, where each **source/drain region** serves as a **source**/drain for four different **non-volatile memory** transistors.

DETAILED DESCRIPTION - A **non-volatile memory** array comprising 2-bit **non-volatile memory** transistors arranged in rows extending along a first axis and columns extending along a second axis perpendicular to the first axis, comprises:

(i) field isolation regions (301-308) in a **semiconductor substrate**; word lines (310-312) extending over the substrate along the first axis, where the word lines form **control gates** of the 2-bit **non-volatile memory** transistors; and

(ii) H-shaped **source/drain regions** (321-328) defined by the field isolation regions and the word lines, where each **source/drain region** serves as a **source**/drain for four different **non-volatile memory** transistors.

An INDEPENDENT CLAIM is also included for a method of fabricating an array of 2-bit **non-volatile memory** cells, comprising:

(a) forming field isolation regions in a **semiconductor substrate**;

(b) forming a lower **dielectric layer** over the substrate;

(c) forming a **floating gate dielectric layer** over the lower **dielectric layer**;

(d) forming an upper **dielectric layer** over the **floating gate dielectric layer**;

(e) forming a **gate electrode layer** over the upper **dielectric layer**;

(f) patterning the **gate electrode layer**, the upper **dielectric layer** and the **floating gate dielectric layer**, where the **gate electrode** is patterned to form word line/**control gate** structures extending along a first axis, and the **floating gate dielectric layer** is patterned to form **floating gate** structures; and

(g) forming H-shaped **source/drain regions** in the substrate, in alignment with the word line/**control gate** structures and field isolation **regions**, the H-shaped **source /drain regions** having a first conductivity type.

USE - As **non-volatile memory** array.

ADVANTAGE - The memory transistor array exhibits a relatively low source/drain series resistance because the **source/drain regions** are small. It also exhibits a low bit line resistance, enabling the memory transistor array to have a large number of rows. Memory transistors exhibit shallow source/drain junction depth (e.g. less than 0.1 microns). They are able to implement self-aligned salicide on both the word lines and the **source/drain regions**. The use of self-aligned salicide results in low resistive/**capacitive** (RC) delay and high-speed operation. Since field isolation regions are used to isolate the H-shaped **source/drain regions**, there is minimal leakage between adjacent **source/drain regions** in memory transistor array.

DESCRIPTION OF DRAWING(S) - The figure is a layout diagram of a portion of a **nonvolatile memory** transistor array that implements H-shaped **source/drain regions**.

Field isolation regions (301-308)
Word lines (310-312)
Source/drain regions (321-328)
pp; 23 DwgNo 3/18

38/3,AB/3 (Item 3 from file: 350)
DIALOG(R)File 350:Derwent WPIX

015430874
WPI Acc No: 2003-493016/200346
XRAM Acc No: C03-131856
XRPX Acc No: N03-391678

Formation of **semiconductor** device comprises covering **surface** of first gate with **protective film** that hardly can be etched by etchant during patterning of second gate

Patent Assignee: MATSUSHITA DENKI SANGYO KK (MATU); MATSUSHITA ELECTRIC IND CO LTD (MATU)
Inventor: DOI H; MIMURO K; OKUDA Y
Number of Countries: 002 Number of Patents: 002
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 20030082878	A1	20030501	US 2002271879	A	20021015	200346	B
JP 2003133443	A	20030509	JP 2001332563	A	20011030	200346	

Priority Applications (No Type Date): JP 2001332563 A 20011030
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 20030082878	A1		19	H01L-021/336	
JP 2003133443	A		10	H01L-021/8247	

Abstract (Basic): US 20030082878 A1
Abstract (Basic):

NOVELTY - The formation of a semiconductor device comprises forming a **non-volatile semiconductor memory** in a first region of a substrate of the device; and forming a semiconductor device in a second region of the substrate. During patterning of a second gate, a surface of a first gate is covered with a **protective film** that hardly can be etched by an etchant used for patterning the gate.

DETAILED DESCRIPTION - The formation of a semiconductor device comprises forming a **non-volatile semiconductor memory** in a first region (Rmem) of a substrate of the device, the **non-volatile semiconductor memory** comprising a first gate (19) that comprises a **tunnel insulating film** (4a), **floating gate electrode** (5a), **capacitor insulating film** (6a), and **control gate electrode** (9a); and forming a semiconductor device in a second region (Rlogic) of the substrate, the device comprising a second gate that comprises a gate **insulating film** and a **gate electrode**. During patterning of a second gate, a surface of a first gate is covered with a **protective film** that hardly can be etched by an etchant used for patterning of the second gate.

USE - Used for manufacturing a semiconductor device.

ADVANTAGE - The process prevents, when patterning a **gate electrode** of a semiconductor device, a **gate electrode** of a **non-volatile semiconductor memory** that has been already patterned from having an abnormal shape and reducing the

chances that the surfaces of high concentration **source** and **drain regions** of the **non-volatile semiconductor memory** may be worn away to cause reduction and fluctuation in a transistor current.

DESCRIPTION OF DRAWING(S) - The figure is a cross-sectional view illustrating a step in the manufacture of a semiconductor device.

Tunnel insulating film (4a)
Floating gate electrode (5a)
Capacitor insulating film (6a)
Control gate electrode (9a)
First gate (19)
First region (Rmem)
Second region (Rlogic)
pp; 19 DwgNo 1A/12

38/3,AB/4 (Item 4 from file: 350)
DIALOG(R)File 350:Derwent WPIX

013430918
WPI Acc No: 2000-602861/200058
XRAM Acc No: C00-180549
XRPX Acc No: N00-446052

Semiconductor memory, especially **non-volatile memory** with ferroelectric **capacitors**, has **source-drain region** formed before producing gate in trench self-aligned with the **source-drain region**

Patent Assignee: SHARP KK (SHAF)
Inventor: ISHIHARA K; KIJIMA T; MIYOSHI T
Number of Countries: 004 Number of Patents: 006
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
DE 10008580	A1	20000907	DE 1008580	A	20000224	200058	B
JP 2000252372	A	20000914	JP 9949397	A	19990226	200060	
KR 2000062649	A	20001025	KR 20009527	A	20000225	200124	
US 6335550	B1	20020101	US 2000513084	A	20000225	200207	
DE 10008580	C2	20020801	DE 1008580	A	20000224	200252	
KR 375750	B	20030315	KR 20009527	A	20000225	200352	

Priority Applications (No Type Date): JP 9949397 A 19990226
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
DE 10008580	A1		13	H01L-027/105	
JP 2000252372	A		10	H01L-021/8247	
KR 2000062649	A			H01L-027/105	
US 6335550	B1			H01L-029/76	
DE 10008580	C2			H01L-027/115	
KR 375750	B			H01L-027/105	Previous Publ. patent KR 2000062649

Abstract (Basic): DE 10008580 A1
Abstract (Basic):

NOVELTY - A semiconductor memory, comprising a **source/drain region** (5) formed before producing a gate (8a, 9a, 10a) in a trench (7) self-aligned with the **source/drain region**, is new.

DETAILED DESCRIPTION - A semiconductor component comprises a **source/drain region** (5) formed in a **semiconductor substrate** (1) of opposite conductivity type, an **interlayer insulation** (6) formed on the substrate and

including a trench (7) which is self-aligned with the **source/ drain region** and which extends down to the substrate surface, and a gate (8a, 9a, 10a) formed on at least the inner wall of the trench.

An INDEPENDENT CLAIM is also included for production of a semiconductor memory as described above. Preferred Features: The **gate** comprises a **dielectric gate** buffer **film** (8a), a ferroelectric gate film (9a) and a **gate electrode** (10a).

USE - Especially as a **non-volatile semiconductor memory** with ferroelectric **capacitors,** e.g. of the type described in JP-A-8-55918.

ADVANTAGE - The design permits production of the **source/ drain region** before the gate, allows formation of a high quality, crack-free ferroelectric gate film in self-alignment with the **source/drain region,** avoids diffusion of constituent elements of the ferroelectric material into the substrate, prevents increase in leakage current and allows production of a highly integrated memory with reduced component dimensions.

DESCRIPTION OF DRAWING(S) - The drawing shows a semiconductor memory according to the invention.

p-**Semiconductor substrate** (1)
Field oxide (2)
Cover oxide (3)
Source/drain region (5)
Interlayer insulations (6, 11)
Trench (7)
Dielectric gate buffer **film** (8a)
Ferroelectric gate film (9a)
Gate electrode (10a)
Source/drain electrode (12)
pp; 13 DwgNo 2E/7

38/3,AB/5   (Item 5 from file: 350)
DIALOG(R)File 350:Derwent WPIX

012903044
WPI Acc No: 2000-074880/200007
XRAM Acc No: C00-021659
XRPX Acc No: N00-058755

Semiconductor memory device e.g., dynamic random access memory **capacitor** and its manufacture

Patent Assignee: MATSUSHITA ELECTRONICS CORP (MATE); JUDAI Y (JUDA-I); NAKAO K (NAKA-I); NOMA A (NOMA-I); SASAI Y (SASA-I); MATSUSHITA ELECTRIC IND CO LTD (MATU)
Inventor: JUDAI Y; NAKAO K; NOMA A; SASAI Y
Number of Countries: 030 Number of Patents: 007
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
EP 969506	A2	20000105	EP 99112857	A	19990702	200007	B
CN 1241036	A	20000112	CN 99109287	A	19990625	200022	
JP 2000082683	A	20000321	JP 99181608	A	19990628	200025	
KR 2000011357	A	20000225	KR 9925573	A	19990630	200102	
TW 412752	A	20001121	TW 99110862	A	19990628	200121	
US 20010023129	A1	20010920	US 99345495	A	19990701	200156	
US 6498094	B2	20021224	US 99345495	A	19990701	200303	

Priority Applications (No Type Date): JP 98188660 A 19980703
Patent Details:

```
Patent No  Kind Lan Pg   Main IPC    Filing Notes
EP 969506     A2 E  22 H01L-021/8242
   Designated States (Regional): AL AT BE CH CY DE DK ES FI FR GB GR IE IT
   LI LT LU LV MC MK NL PT RO SE SI
CN 1241036    A        H01L-027/108
JP 2000082683 A     14 H01L-021/28
KR 2000011357 A        H01L-027/108
TW 412752     A        H01B-003/12
US 20010023129 A1       H01L-021/8242
US 6498094    B2       H01L-021/4763
```

Abstract (Basic): EP 969506 A2
Abstract (Basic):

NOVELTY - A semiconductor element (17) and a **capacitor** (28) are electrically connected to each other via a plug (21) within the contact hole (19a). The plug (21) consists of a conductive film containing a platinum group element.

DETAILED DESCRIPTION - A **semiconductor** device comprises: a **substrate** (11) formed with a semiconductor element (17); an **insulating film** (19) formed on the substrate (11), the **insulating film** (19) having a connection hole (19a) and covering the semiconductor element (17); an underlying conductive film (20) formed in at least a lower part of the connection hole (19a) and electrically connected to the semiconductor element (17); and a conductive film (21) formed in an upper part of the connection hole (19a) and containing a platinum group element.

INDEPENDENT CLAIMS are also included for the following: (a) a **semiconductor** device comprising: a **substrate** formed with a **semiconductor** element; an **insulating film** formed on the substrate, the **insulating film** having a connection hole and covering the semiconductor element; a conductive film formed in an upper part of the connection hole and containing a platinum group element; and a barrier layer formed in a lower part of connection hole. The barrier layer has conductivity, is electrically connected to the semiconductor element and prevents a constituent element of the conductive film from being diffused into the substrate; (b) methods of manufacturing semiconductor devices.

USE - Semiconductor memory devices e.g., DRAM (dynamic random access memory) **capacitors**. If the **dielectric film** is made of a ferroelectric, a **nonvolatile memory** device can be implemented.

ADVANTAGE - Excellent electric connection is maintained among the underlying conductive film, conductive film and the semiconductor element, which improves the reliability of the device. If a transistor is used as the semiconductor element, a semiconductor memory device having excellent conduction between transistor and **capacitor** can be implemented. Since the upper end of the conductive film as the plug is used as the lower electrode of the **capacitor** without any alteration, the step of forming the lower electrode of the **capacitor** can be omitted and the size of the **capacitor** formed is reduced.

DESCRIPTION OF DRAWING(S) - The diagram illustrates a cross sectional view of the semiconductor memory device.

Substrate (11)
Isolation film (12)
Gate insulating film (13)
Gate electrode (14)
Drain region (15)
Source region (16)
Transistor (17)

Bit line (18)
Insulating film (19)
Contact hole (19a)
Underlying conductive film (20)
Plug (21)
Capacitor (28)
Lower electrode (25)
Insulating film (26)
Upper electrode (27)
pp; 22 DwgNo 2/9

38/3,AB/6 (Item 6 from file: 350)
DIALOG(R)File 350:Derwent WPIX

012623460
WPI Acc No: 1999-429564/199936
XRPX Acc No: N99-319748
Single level gate **nonvolatile memory** device for use in high density integrated circuit
Patent Assignee: MOTOROLA INC (MOTI)
Inventor: BUXO J; CARMAN E S; NGUYEN Q X; PAGES I M; PARRIS P M; SEE Y; SICARD T M
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 5929478	A	19990727	US 97886746	A	19970702	199936	B

Priority Applications (No Type Date): US 97886746 A 19970702
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 5929478	A		11	H01L-029/76	

Abstract (Basic): US 5929478 A
Abstract (Basic):

NOVELTY - Major portion of a semiconductor layer (22) with preset concentration, formed on a substrate (21), faces away from an interface (24) formed between the layer and the substrate. **Source** and **drain regions** (41,42) are formed in wells (27) to define channel region (51). A conductive layer (36) is laid over **dielectric layers** (34,35) formed over the wells, to form gate of the FET.

DETAILED DESCRIPTION - The single level gate NVM device (20) includes a **floating gate** FET (11) and a **capacitor** (12) fabricated in two P-wells (27,28) formed in an N-epitaxial layer (22) on a P-substrate (21). P+ sinkers (29,31) and N-type buried layers (25,26) provide isolation between the two P-wells. The NVM device is programmed or erased by biasing the FET and the **capacitor** to move charge carriers onto or away from a conductive layer (36) which serves as a **floating gate** (14) of the FET. Data is read from the NVM device by sensing a current flowing in the FET while applying a reading voltage to the **capacitor**.

USE - For use in high density integrated circuits.

ADVANTAGE - Simple and cost effective **nonvolatile memory** is achieved by providing easy fabrication involving different dopant concentration.

DESCRIPTION OF DRAWING(S) - The figure depicts the cross-sectional view of single level gate NVM.

Semiconductor substrate (21)

```
        Semiconductor layer (22)
        Interface (24)
        Wells (27)
        P-type sinkers (29,31)
        Dielectric layers (34,35)
        Conductive layer (36)
        Source and drain regions (41,42)
        Channel region (51)
        pp; 11 DwgNo 2/5


 38/3,AB/7     (Item 7 from file: 350)
DIALOG(R)File 350:Derwent WPIX
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012219815
WPI Acc No: 1999-025921/199903
XRAM Acc No: C99-008143
XRPX Acc No: N99-019900
  Non-volatile semiconductor memory cell -
  especially contact-free MOS memory cell with high capacitive
  coupling between floating and control gates
Patent Assignee: LG SEMICON CO LTD (GLDS  ); GOLDSTAR ELECTRON CO LTD (GLDS
  ); HYUNDAI MICROELECTRONICS CO LTD (HYUN-N)
Inventor: RA K; LA K; RAH G M; RA K M
Number of Countries: 006  Number of Patents: 008
Patent Family:
Patent No     Kind   Date     Applicat No    Kind   Date     Week
DE 19822523    A1  19981203  DE 1022523       A   19980519  199903  B
JP 10335611    A   19981218  JP 9854981       A   19980306  199910
CN 1200574     A   19981202  CN 98109306      A   19980526  199916
KR 98084835    A   19981205  KR 9720735       A   19970526  200008
US 6037226     A   20000314  US 9879445       A   19980515  200020
TW 392356      A   20000601  TW 98101484      A   19980205  200060
KR 232200      B1  19991201  KR 9720735       A   19970526  200111
US 6335553     B1  20020101  US 9879445       A   19980515  200207
                             US 2000499381    A   20000207

Priority Applications (No Type Date): KR 9720735 A 19970526
Patent Details:
Patent No  Kind Lan Pg   Main IPC    Filing Notes
DE 19822523   A1    33 H01L-027/115
JP 10335611   A     11 H01L-027/115
CN 1200574    A        H01L-027/105
KR 98084835   A        H01L-027/115
US 6037226    A        H01L-021/8247
TW 392356     A        H01L-029/772
KR 232200     B1       H01L-027/115
US 6335553    B1       H01L-029/76   Div ex application US 9879445
                                     Div ex patent US 6037226

Abstract (Basic): DE 19822523 A
        A non-volatile semiconductor memory cell
    has (a) a common second conductivity type source region
    (32a) located between and spaced from first and second, second
    conductivity type drain regions in a first direction within
    a first conductivity type semiconductor substrate (31); (b)
    an insulating island (40b) provided on an insulating film
    (38a, 39) on the substrate in a zone above and at the second
    drain region side of the common source region;
```

(c) a first **floating gate** (35a) located on the **insulating film** at the first **drain region** side of the common **source region** and contiguous with the insulating island; (d) a second **floating gate** on the first **floating gate** and on the **insulating** island; (e) a **dielectric film** (36) on the exposed surfaces of the first and second **floating gates;** and (f) a **control gate** (37) in a second direction on the **dielectric film** on the second **floating gate.** Also claimed are a similar **non-volatile semiconductor memory** cell with a single **floating gate, non-volatile semiconductor** components having matrices of such memory cells and processes for producing these components.

USE - Especially as a contact-free, **non-volatile** MOS **memory** cell.

ADVANTAGE - The cell design allows high **capacitive coupling** between the **floating gate**(s) and the **control gate.**

Dwg.8/16

38/3,AB/8   (Item 8 from file: 350)
DIALOG(R)File 350:Derwent WPIX

009967252
WPI Acc No: 1994-234965/199428
Related WPI Acc No: 1994-117876
XRPX Acc No: N94-185699

Non-volatile semiconductor memory cell with **floating gate** - has two **control gates,** one beneath part of **floating gate**

Patent Assignee: YU S (YUSS-I)
Inventor: YU S
Number of Countries: 019 Number of Patents: 007
Patent Family:

```
Patent No     Kind   Date     Applicat No    Kind   Date      Week
WO 9415363     A1  19940707  WO 93US12485    A   19931220  199428  B
US 5394357     A   19950228  US 9324258      A   19930301  199514
EP 676088      A1  19951011  WO 93US12485    A   19931220  199545
                             EP 94907098     A   19931220
JP 7509813     W   19951026  WO 93US12485    A   19931220  199551
                             JP 94515414     A   19931220
US 5723888     A   19980303  US 9362237      A   19930517  199816
EP 676088      A4  19970101  EP 94907098     A   19931220  199841
US 5859455     A   19990112  US 92999609     A   19921231  199910
```

Priority Applications (No Type Date): US 9362237 A 19930517; US 92997236 A 19921228; US 92999609 A 19921231; US 9324258 A 19930301

Patent Details:

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Patent No  Kind Lan Pg   Main IPC     Filing Notes
WO 9415363    A1 E  40 H01L-027/10
   Designated States (National): JP
   Designated States (Regional): AT BE CH DE DK ES FR GB GR IE IT LU MC NL
   PT SE
US 5394357    A     10 G11C-011/34
EP 676088     A1 E  40 H01L-027/10   Based on patent WO 9415363
   Designated States (Regional): AT BE CH DE DK ES FR GB GR IE IT LI LU MC
   NL PT SE
JP 7509813    W     11 H01L-021/8247 Based on patent WO 9415363
```

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US 5723888    A     10 H01L-029/76
EP 676088     A4       H01L-027/10
US 5859455    A        H01L-029/788
```

Abstract (Basic): WO 9415363 A

The **non-volatile memory** cell (2) includes a **floating gate** (16) with a segment between two **control gates** (12,14) and another segment over part of the channel. Addressing of the memory cell (2) for programming, de-programming and reading involves the simultaneous energisation of both the **control gates**. The energisation of one but not both **control gates** cannot activate the memory cell.

A memory cell array comprises the memory cells arranged in a matrix format. Addressing of each of the cells in the array is simply the simultaneous energisation of a pair of **control gates** perpendicularly criss-crossing the underlying memory cell.

ADVANTAGE - Rapid random addressing.

Dwg.2/39

Abstract (Equivalent): US 5723888 A

The **non-volatile memory** cell (2) includes a **floating gate** (16) with a segment between two **control gates** (12,14) and another segment over part of the channel. Addressing of the memory cell (2) for programming, de-programming and reading involves the simultaneous energisation of both the **control gates**. The energisation of one but not both **control gates** cannot activate the memory cell.

A memory cell array comprises the memory cells arranged in a matrix format. Addressing of each of the cells in the array is simply the simultaneous energisation of a pair of **control gates** perpendicularly criss-crossing the underlying memory cell.

ADVANTAGE - Rapid random addressing.

Dwg.8/8

US 5394357 A

The **non-volatile memory** cell comprises a **semiconductor substrate** of a first conductivity type. A source is formed in the **semiconductor substrate**. A drain is formed in the **semiconductor substrate** and spaced from the **source**. A diffusion **region** of a second conductivity type is formed in the **semiconductor substrate** and between the source and the drain. Channels are formed between the diffusion **region** and the **drain**, and between the diffusion **region** and the **source**.

A first **control gate** is **dielectrically** disposed atop the diffusion region. A **floating gate** is **dielectrically** disposed atop the first **control gate** and the channels. A second **control gate** is **dielectrically** disposed atop the **floating gate**.

USE/ADVANTAGE - For large scale integration applications in which memory cells are arranged in NAND structure. Memory cell can only be addressed for programming or deprogramming by simultaneous energisation of two **control gates**. With this unique feature, any memory cell in memory array can be randomly accessed. Moreover, two **control gates** associated with each of **floating gate** also increase **coupling capacitances**, thereby speeding up operations.

Dwg.3b/7

38/3,AB/9   (Item 9 from file: 350)
DIALOG(R)File 350:Derwent WPIX

008820513
WPI Acc No: 1991-324526/199144
XRAM Acc No: C91-140181
XRPX Acc No: N91-248827

Floating gate transistor mfr. - provides IC **capacitor** for ADC and memory devices, and uses low-temp. processing and one level of polysilicon

Patent Assignee: TEXAS INSTR INC (TEXI)
Inventor: PATERSON J L
Number of Countries: 008 Number of Patents: 007
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 5057447	A	19911015	US 90549862	A	19900709	199144	B
EP 466016	A	19920115	EP 91111041	A	19910703	199203	
JP 4233279	A	19920821	JP 91166862	A	19910708	199240	
EP 466016	A3	19930915	EP 91111041	A	19910703	199509	
EP 466016	B1	19961127	EP 91111041	A	19910703	199701	
DE 69123295	E	19970109	DE 623295	A	19910703	199707	
			EP 91111041	A	19910703		
KR 208846	B1	19990715	KR 9111533	A	19910708	200066	

Priority Applications (No Type Date): US 90549862 A 19900709
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 466016	A				
Designated States (Regional): DE FR GB IT NL					
JP 4233279	A		9	H01L-029/788	
EP 466016	B1	E	17	H01L-029/788	
Designated States (Regional): DE FR GB IT NL					
DE 69123295	E			H01L-029/788	Based on patent EP 466016
KR 208846	B1			H01L-027/04	

Abstract (Basic): US 5057447 A

A silicide/nitride method for making a **floating-gate** transistor at a **semiconductor** body **surface** comprising forming a field **dielectric** structure to define an uncovered moat **region** in which **source** and drain diffusions are formed, forming a poly-Si **floating gate** (10) having a **capacitor** bottom plate over the field **dielectric** and a **gate** between source and drain. An overall multilevel **dielectric layer** (16) is formed, part of which is removed to expose part of the **capacitor** plate, and a silicide film (14) formed on this bottom plate. A **capacitor dielectric** is formed (20,22) and partly removed to expose the moat region, and a patterned metal layer (24,30) formed to give a **capacitor** top plate and to contact source and/or drain.

USE/ADVANTAGE - A method of making a **floating gate** transistor (claimed) is provided which is useful in high-density Analog-to-digital converters (ADC) and **non-volatile memory** circuits. The IC **capacitor** has a silicided poly-Si bottom plate and requires only low-temp. processing, only one level of poly-Si and has a low voltage coefft. of **capacitance**. (12pp Dwg.No.2/3)

Abstract (Equivalent): EP 466016 B

A **floating-gate** transistor formed at a **surface** of a **semiconductor** body (4), comprising a source diffusion (42), a drain diffusion (40), and a **floating-gate** (10), comprising polycrystalline silicon, wherein a field **dielectric** (8) is provided at said **surface** of the **semiconductor** body (4) to

define a moat region not covered by said field **dielectric** (8), wherein said source diffusion (42) is provided at a first portion of said moat **region**, wherein said **drain** diffusion (40) is provided at a second portion of said moat region, wherein said **floating-gate** (10) has a **capacitor** bottom plate section disposed over said field **dielectric** (8) and has a gate portion extending off of said field **dielectric** (8) and disposed between said source and drain diffusions (40, 42), wherein a multilevel **dielectric** (16) is disposed over said **semiconductor** body **surface** away from said **capacitor** bottom plate section, wherein a silicide film (14) is disposed on only a portion of a top surface of said **capacitor** bottom plate section (10), wherein a **capacitor dielectric layer** (20, 22) is disposed over and in contact with said silicide **film** (14) at said **capacitor** bottom plate section and is disposed over said multilevel **dielectric** (16) away from said **capacitor** bottom plate section, and wherein a patterned conductor layer (24, 30), comprising a metal layer, has a first portion, comprising a metal layer, has a first portion, comprising a **control gate** disposed over and in contact with said **capacitor dielectric layer** (20, 22) at said **capacitor dielectric layer** (20, 22) at said **capacitor** bottom plate section, and a second portion disposed over and in contact with at least one of said source diffusion (42) and said drain diffusion (40).

(Dwg.1/4

38/3,AB/10 (Item 1 from file: 347)
DIALOG(R)File 347:JAPIO
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07639589
MANUFACTURING METHOD OF SEMICONDUCTOR DEVICE

PUB. NO.: 2003-133443 [JP 2003133443 A]
PUBLISHED: May 09, 2003 (20030509)
INVENTOR(s): MIMURO KEN
DOI HIROYUKI
OKUDA YASUSHI
APPLICANT(s): MATSUSHITA ELECTRIC IND CO LTD
APPL. NO.: 2001-332563 [JP 2001332563]
FILED: October 30, 2001 (20011030)

ABSTRACT

PROBLEM TO BE SOLVED: To provide a manufacturing method of a semiconductor device for obtaining a satisfactory semiconductor device that prevents the generation of abnormality in the shape of the **gate electrode** of a **non-volatile semiconductor** device by an etching process, and prevents the scrape of the surface of the high-concentration **source** and **drain regions** of the **non-volatile semiconductor** storage.

SOLUTION: The manufacturing method of the semiconductor device comprises a first process for forming a **non-volatile semiconductor** storage that has a first gate consisting of a **tunnel insulating film**, a stray **gate** electrode, a **capacity insulating film**, and a **control gate electrode** in a first region on a **semiconductor substrate**, and a second process for forming a semiconductor storage that has a second gate consisting of the gate **insulating film** and **gate electrode** in a second region on the **semiconductor**

substrate . In this case, when the second gate is subjected to patterning, the surface of the first gate is **coated** with a **protection film** that cannot be etched by an etching material used for the patterning of the second gate.

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38/3,AB/11 (Item 2 from file: 347)
DIALOG(R)File 347:JAPIO
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06309864
NONVOLATILE SEMICONDUCTOR MEMORY

PUB. NO.: 11-251462 [JP 11251462 A]
PUBLISHED: September 17, 1999 (19990917)
INVENTOR(s): HATAKEYAMA KAZUO
APPLICANT(s): TOSHIBA CORP
APPL. NO.: 10-053323 [JP 9853323]
FILED: March 05, 1998 (19980305)

ABSTRACT

PROBLEM TO BE SOLVED: To enable the cost reduction per **memory capacity** by providing **nonvolatile memory** cells between bit lines and source lines and conductive gates via an oxide film on the source lines to reduce the area per bit.

SOLUTION: P-type well regions 11 are formed on an n-type **semiconductor substrate** 10, and an NAND cell composed of eight memory cells is disposed on the p-type well region 11. Each memory cell constitutes a laminate structure of a **floating gate** 15, a second **gate insulation film** 16 and **control gate** 17 through a first **insulation film** (**tunnel oxide film**) 14, adjacent cells of the series arranged memory cells commonly have an n-type diffused layer as source-drains, the **control gate** 17 functions as a common word line in the row direction, and a drain side selective gate 18D is disposed at one end of the NAND cell via an n-type diffused layer. At the other end a **source region** 13T exists, and a conductive gate 22 is disposed on the **source region** 13T.

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38/3,AB/12 (Item 3 from file: 347)
DIALOG(R)File 347:JAPIO
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04175380
NON-VOLATILE SEMICONDUCTOR MEMORY CELL

PUB. NO.: 05-167080 [JP 5167080 A]
PUBLISHED: July 02, 1993 (19930702)
INVENTOR(s): KAWASHIMA HIROMI
APPLICANT(s): FUJITSU LTD [000522] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 03-331039 [JP 91331039]
FILED: December 16, 1991 (19911216)
JOURNAL: Section: E, Section No. 1448, Vol. 17, No. 570, Pg. 12,

October 15, 1993 (19931015)

ABSTRACT

PURPOSE: To provide a **non-volatile semiconductor memory** cell of a structure suitable for large **capacity** memories by reducing a required area per cell by disposing vertically a memory transistor and a selection transistor.

CONSTITUTION: A **source region** 11 and a **drain region** 12 are formed in a **semiconductor substrate**, and a **floating gate** 14 is disposed above the **drain region** through a **tunnel insulating film**. A first **control gate** 16 is further disposed above the **floating gate** 14 through an **insulating film**, and a silicon 18 is disposed above the **floating gate** 16 through an **insulating film**, in which silicon 18 a band-shaped part 19 is formed. Further, a one conductivity type impurity is introduced into a region which traverses the band-shaped part with a predetermined fine width, and an another conductivity type impurity is introduced into two regions in contact with the traversing region. A second **control gate** 21 is disposed through an **insulating film** on the upper portions of the traversing region into which the one conductivity type impurity is introduced and of the two regions into which the another conductivity type impurity is introduced. Further, one of the two regions is electrically connected with the **drain region**.

38/3,AB/13 (Item 4 from file: 347)
DIALOG(R)File 347:JAPIO
(c) 2004 JPO & JAPIO. All rts. reserv.

03246675
MANUFACTURE OF **SEMICONDUCTOR NONVOLATILE MEMORY**

PUB. NO.: 02-222175 [JP 2222175 A]
PUBLISHED: September 04, 1990 (19900904)
INVENTOR(s): NAKANISHI AKISHIGE
APPLICANT(s): SEIKO INSTR INC [000232] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 01-042606 [JP 8942606]
FILED: February 22, 1989 (19890222)
JOURNAL: Section: E, Section No. 1003, Vol. 14, No. 524, Pg. 106, November 16, 1990 (19901116)

ABSTRACT

PURPOSE: To manufacture a semiconductor memory having a high film quality and high reliability of **tunnel insulating film** itself having an approximately constant current value by suppressing the temperature of a heat treatment process after the formation of a **gate insulating film** at a specific value or below and suppressing a gate threshold-voltage rise due to a MOSFET electron trap.
CONSTITUTION: Channel injection write is executed to a poly Si **electrode** formed as a **floating** 5 through a **gate insulating film** 2 on a channel region. A tunnel is erased from the gate 5 by utilizing the tunnel currents of the thin **gate insulating film** 2 in approximately 100 angstroms shaped onto a tunnel **drain region** 3 in the region 3 formed to the **surface** section of a **semiconductor substrate** 1, thus manufacture a **semiconductor non-volatile memory**. An oxide film deposited through the high-temperature chemical vapor growth

method of $SiHCl_2$ and N_2O at a high-treatment process temperature of 800 deg.C or more after the formation of the **insulating film** 2 is used as a **capacitor** oxide **film** on the gate 6 at that time, thus inhibiting a heat treatment process after the formation of the **gate insulating film** at 950 deg.C or less, then acquiring the memory having high film quality of a **tunnel insulating film** in approximately 100 angstroms .

43/3,AB/1 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX

015997418
WPI Acc No: 2004-155268/200415
XRAM Acc No: C04-061786
XRPX Acc No: N04-124183

Nonvolatile semiconductor memory device, comprises semiconductor layer including **source region**, channel **region** and **drain region** of memory cell, and lower **insulator film** located between **substrate** and **semiconductor** layer

Patent Assignee: MITSUBISHI ELECTRIC CORP (MITQ); RUNESASU TECHNOLOGY KK (RUNE-N); MITSUBISHI DENKI KK (MITQ); KATO H (KATO-I); KUGE S (KUGE-I); MORISHITA F (MORI-I); NODA H (NODA-I); UENO S (UENO-I)
Inventor: KATO H; KUGE S; MORISHITA F; NODA H; UENO S
Number of Countries: 004 Number of Patents: 004
Patent Family:

```
Patent No       Kind   Date     Applicat No     Kind   Date      Week
US 20040007734  A1   20040115  US 2002330093   A    20021230  200415  B
JP 2004039965   A    20040205  JP 2002197062   A    20020705  200415
CN 1467851      A    20040114  CN 2003120161   A    20030310  200423
KR 2004004041   A    20040113  KR 200314771    A    20030310  200434
```

Priority Applications (No Type Date): JP 2002197062 A 20020705
Patent Details:

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Patent No  Kind Lan Pg   Main IPC     Filing Notes
US 20040007734 A1    27 H01L-029/788
JP 2004039965 A     25 H01L-021/8247
CN 1467851    A        H01L-027/105
KR 2004004041 A        H01L-029/788
```

Abstract (Basic): US 20040007734 A1

Abstract (Basic):

NOVELTY - A **nonvolatile semiconductor memory** device including a memory cell, comprises:

(a) a **semiconductor substrate** (1);

(b) a semiconductor layer, located above the **semiconductor substrate**, including a **source region** (4), a channel **region** and a **drain region** (5) of the memory cell; and

(c) a lower **insulator film** (2) located between the **semiconductor substrate** and the **semiconductor** layer.

USE - **Nonvolatile semiconductor memory** device including memory cell.

ADVANTAGE - The device is capable of storing information of four bits in one memory cell. It is also capable of ensuring a desired threshold voltage distribution margin between an erased state and a written state of memory cell.

DESCRIPTION OF DRAWING(S) - The figure is a section of a **memory** cell of a **nonvolatile semiconductor memory** device.

Semiconductor substrate (1)
Insulator film (2)
Source region (4)
Drain region (5)
Gate electrode (7)
pp; 27 DwgNo 1/29

43/3,AB/2 (Item 2 from file: 350)
DIALOG(R)File 350:Derwent WPIX

014434879
WPI Acc No: 2002-255582/200230
Related WPI Acc No: 2003-209660; 2004-293258
XRAM Acc No: C02-076194
XRPX Acc No: N02-197633

Non-volatile semiconductor memory device includes control **gate**, control **gate insulating layer**, **insulating layers**, **drain region**, **source region**, and **floating gate**

Patent Assignee: HYNIX SEMICONDUCTOR INC (HYNI-N)
Inventor: KIM H J; KIM H
Number of Countries: 002 Number of Patents: 004
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 20020018364	A1	20020214	US 2001863448	A	20010524	200230	B
KR 2001107127	A	20011207	KR 200028366	A	20000525	200236	
US 6501124	B2	20021231	US 2001863448	A	20010524	200305	
KR 390889	B	20030710	KR 200028366	A	20000525	200409	

Priority Applications (No Type Date): KR 200028366 A 20000525
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 20020018364	A1		16	G11C-011/34	
KR 2001107127	A			H01L-027/115	
US 6501124	B2			H01L-029/788	
KR 390889	B			H01L-027/115	Previous Publ. patent KR 2001107127

Abstract (Basic): US 20020018364 A1
Abstract (Basic):

NOVELTY - A **non-volatile semiconductor memory** device consists of a **semiconductor substrate**, a **control gate**, a **control gate insulating layer**, a first **insulating layer**, a **drain region**, a **source region**, a second **insulating layer**, and a **floating gate**.

DETAILED DESCRIPTION - A **non-volatile semiconductor memory** device includes:

(a) a **semiconductor substrate** including a device active area and a device isolation area (700);

(b) a **control gate** (62) formed on the device active area, and dividing the device active area into a first region and a second region;

(c) a **control gate insulating layer** formed between the substrate and the **control gate;**

(d) a first **insulating layer** covering a top surface and a side of the **control gate;**

(e) a **drain region** (67) formed in the first region of the substrate;

(f) a **source region** (72) formed in the second region of the substrate, and separated from the **control gate;**

(g) a second **insulating layer** formed on the second **region** between the **source region** and the **control gate**, and formed on a portion of a surface of the first region adjacent the first **insulating layer** and over the **drain region**; and

(h) a **floating gate** (69) covering the second and first

insulating layers.

INDEPENDENT CLAIMS are also included for:

(A) a method of fabricating the **non-volatile semiconductor memory** device, comprises:

(i) forming a **control gate** on a portion of a memory cell area of a **semiconductor substrate**, in which the memory cell area, which is divided into a first region and a second region by the **control gate**, is defined by a device isolation layer;

(ii) providing a **control gate insulating layer** between the **control gate** and the **semiconductor substrate**; forming a first **insulating layer** on an exposed surface of the **control gate**;

(iii) forming a **drain region** in the first region;

(iv) forming a third **insulating layer** covering portions of the second **region** and the **drain region**, in which the third **insulating layer** is extended from the first **insulating layer**;

(v) forming a **floating gate** on the third **insulating layer** and on an exposed surface of the first **insulating layer**; and

(vi) forming a **source region** in the second region, in which the **floating gate** does not overlap the **source region**; and

(B) a method of preventing disturbance of a **non-volatile semiconductor memory**, comprises:

(1) providing a **non-volatile semiconductor memory** device including memory cells each of which includes a **control gate**, a drain junction, a source junction, a **floating gate**, a word line, and a bit line;

(2) generating a first electric charge of a first parasitic **capacitance** from an applied **control gate** voltage and a **floating gate** voltage as a function of the first parasitic **capacitance** with respect to the difference between the **control gate** voltage and the **floating gate** voltage;

(3) generating a third electric charge of a third parasitic **capacitance** from a source voltage at the source junction and the induced **floating gate** voltage as a function of the third parasitic **capacitance** with respect to the difference between the source voltage and the **floating gate** voltage;

(4) generating a fourth electric charge of a fourth parasitic **capacitance** from a bulk substrate voltage and the induced **floating gate** voltage as a function of the fourth parasitic **capacitance** with respect to the difference between the bulk substrate voltage and the **floating gate** voltage;

(5) generating a second electric charge of a second parasitic **capacitance** from a drain voltage at the drain junction and the induced **floating gate** voltage as a function of the second parasitic **capacitance** with respect to the difference between the drain voltage and the **floating gate** voltage;

(6) selecting one of the **control gate** voltage and the drain voltage to reduce disturbance at the word line and the bit line where the **floating gate** voltage is determined by the **capacitance** of the of the first and second parasitic **capacitors**, the **control gate** voltage, the drain voltage, and the total parasitic **capacitance**; and

(7) programming the **non-volatile semiconductor memory** by F-N tunneling or erasing by discharging electrons.

USE - Used as a **non-volatile semiconductor memory** device.

ADVANTAGE - The method prevents programming disturbance and enables programming operated by a byte unit by achieving a programming and an erasing of a memory device through a F-N tunneling.

DESCRIPTION OF DRAWING(S) - The figure shows a layout of an electrically erasable and programmable read only memory device in the inventive semiconductor device.

Control gate (62)
Drain region (67)
Floating gate (69)
Source region (72)
Device isolation area (700)
pp; 16 DwgNo 2B/5

43/3,AB/3 (Item 3 from file: 350)
DIALOG(R)File 350:Derwent WPIX

013790947
WPI Acc No: 2001-275158/200129
XRAM Acc No: C01-083593
XRPX Acc No: N01-196686

Non-volatile memory comprising ferroelectric transistor and ferroelectric **capacitor**

Patent Assignee: ROHM CO LTD (ROHL)
Inventor: NAKAMURA T
Number of Countries: 029 Number of Patents: 005
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
EP 1089341	A2	20010404	EP 2000121187	A	20000929	200129	B
JP 2001102465	A	20010413	JP 99280237	A	19990930	200138	
US 6285577	B1	20010904	US 2000671599	A	20000928	200154	
KR 2001030545	A	20010416	KR 200057409	A	20000929	200163	
TW 480490	A	20020321	TW 2000120344	A	20000930	200308	

Priority Applications (No Type Date): JP 99280237 A 19990930
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 1089341	A2	E	10	H01L-027/115	

Designated States (Regional): AL AT BE CH CY DE DK ES FI FR GB GR IE IT LI LT LU LV MC MK NL PT RO SE SI

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
JP 2001102465	A		6	H01L-021/8247	
US 6285577	B1			G11C-011/22	
KR 2001030545	A			H01L-027/115	
TW 480490	A			G11C-014/00	

Abstract (Basic): EP 1089341 A2
Abstract (Basic):

NOVELTY - The transistor includes a **gate electrode** stacked through a 1st ferroelectric layer (6) on the **surface** of a **semiconductor substrate** (1) between **source** and **drain regions** (2,3). The **capacitor** includes two electrodes (16,18) sandwiching a ferroelectric layer 917). The 1st electrode is connected to one of the **source** and **drain regions**.

DETAILED DESCRIPTION - A potential difference is generated between the **gate electrode** and the **semiconductor substrate** to invert the polarization of the 1st ferroelectric layer. A 2nd potential difference is generated between the 1st and 2nd electrode to invert the polarization of the 2nd ferroelectric layer so that write and read of multilevel values are executed.

An INDEPENDENT CLAIM is included for a **non-volatile memory** similar to the above where the **gate electrode** acts as the **capacitor**. The voltages applied to the **electrodes** are independently **controlled**.

USE - Composite **non-volatile memories**.

ADVANTAGE - Executes read and write of multilevel information.

DESCRIPTION OF DRAWING(S) - The diagram shows a **non-volatile memory** as described above.

Substrate (1)
Source/drain regions (2,3)
Gate insulating film (4)
Floating gate (5)
Ferroelectric layer (6)
PZT **control gate** (7)
1st electrode (16)
PZT ferroelectric layer (17)
2nd electrode (18)
Interlayer insulating film (19,20)
pp; 10 DwgNo 2A/10

43/3,AB/4 (Item 4 from file: 350)
DIALOG(R)File 350:Derwent WPIX

011676410
WPI Acc No: 1998-093319/199809
XRAM Acc No: C98-031221
XRPX Acc No: N98-074551

Non-volatile semiconductor memory - consisting of matrix of memory cell arrays comprising MOS transistor and **capacitor** connected in series

Patent Assignee: TOSHIBA KK (TOKE)
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
JP 9321237	A	19971212	JP 96133030	A	19960528	199809	B

Priority Applications (No Type Date): JP 96133030 A 19960528
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
JP 9321237	A		10	H01L-027/108	

Abstract (Basic): JP 9321237 A

A new **non-volatile semiconductor memory** consists of a matrix of memory cell arrays. The memory cell consists of a MOS transistor (Q) and a **capacitor** (C) which are connected in series. The memory is equipped with word lines (WL) bonded to the **gate electrode** of each MOS transistor, plate lines (PL) bonded to the plate electrode of each **capacitors**, bit lines (BL) bonded commonly to the **source** and **drain regions** of the MOS transistors. The **capacitor** is made of a ferroelectric film sandwiched between electrodes. The ferroelectric film is made of a Pb-contg. perovskite cpd. contg. Ho, Co, Cr, Dy, W, Y, V, Sm, or Gd or a Bi-contg. layered cpd. contg. Ho, Co, Cr, Dy, W, Y, V, Sm, or Gd. A new **non-volatile semiconductor memory** is also claimed and consists of a **semiconductor substrate**, **source** and **drain regions** formed on the surface of the substrate, a **gate insulator film** formed on the

source and **drain regions,** the first **electrode** formed on the **gate insulator film,** a ferroelectric **film** formed on the first electrode, and the second electrode formed on the ferroelectric **film.** A new **capacitor** consisting of a ferroelectric film which is formed between the first and second electrodes is also claimed, which memorises data by reversing its polarity. The prodn. of the **capacitor** is also claimed, which comprises the steps: (a) the first electrode is formed; (b) the ferroelectric film is formed at 0-200 deg. C, then the film is crystallised by heating; (c) the second electrode is formed.

USE - For memories of RFID (radio frequency identification) cards, notebook computers, or PDA's (personal data assistant).

ADVANTAGE - The **non-volatile memory** has a higher reliability. It is produced with a higher yield.

Dwg.1/14

43/3,AB/5 (Item 5 from file: 350)
DIALOG(R)File 350:Derwent WPIX

010505829
WPI Acc No: 1996-002780/199601
XRAM Acc No: C96-000771
XRPX Acc No: N96-002523

Non-volatile semiconductor memory - stores data by amplifying change in charge stored in **floating gate** by proportionally increasing channel level

Patent Assignee: SHARP KK (SHAF)
Inventor: ITOH N
Number of Countries: 002 Number of Patents: 002
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
JP 7273228	A	19951020	JP 9457157	A	19940328	199601	B
US 5526308	A	19960611	US 95371008	A	19950110	199629	

Priority Applications (No Type Date): JP 9457157 A 19940328
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
JP 7273228	A		8	H01L-021/8247	
US 5526308	A		16	G11C-013/00	

Abstract (Basic): JP 7273228 A

The **non-volatile semiconductor memory** has a **floating gate** (FG) formed through an **insulation film** on a **semiconductor substrate.** The film couple is a **floating gate** to a **control gate** (CG) **capacitively** on the substrate. Under the **floating gate,** impurity diffusion region of opposite conductivity type is connected on the substrate. The memory cell which is arranged in matrix form has a data line connected to this region.

A control voltage is applied to a **control gate** for read-out in order to raise the **floating gate** potential. Any change in charge stored in **floating gate** channel causes bigger change in **capacitance** of the FG channels and the substrate. This results in difference of potential of the data line and thus generating voltage internally and a read-out is performed.

ADVANTAGE - Eliminates need for **source** diffusion **region** . Reduces chip area. Eliminates need for write-in data associated with read-out. Avoids incorrect read-out.

Dwg.1/13

Abstract (Equivalent): US 5526308 A

A **nonvolatile semiconductor memory** device, comprising:

a **semiconductor substrate;**

an **insulation layer** located on the **semiconductor substrate;**

a plurality of memory cells arranged on the **semiconductor substrate** in a matrix with the **insulation layer** therebetween, the memory cells each including a **floating gate** located on the **semiconductor substrate** with the **insulation layer** therebetween, a **control gate** for forming a **capacitance** with the **floating gate** with the **insulation layer** interposed therebetween, an impurity diffusion region located in the **semiconductor substrate** and having an opposite conductivity to that of the **semiconductor substrate**, and a bit line connected to the impurity diffusion region;

application means for applying a control voltage for reading data from the memory cell to the **control gate;** and

determination means for determining data to be read from a plurality of sets of data and outputting the data, wherein

the determination means determines the data to be read, based on the difference in voltages on the bit line, the difference in the voltages on the bit line which voltage is caused by the difference in the **capacitances** between the **floating gate** and the **semiconductor substrate**, the difference in the **capacitance** being caused by the difference in charge levels in the **floating gate** when the **control** voltage is applied to the **control gate**.

Dwg.4

43/3,AB/6 (Item 6 from file: 350)
DIALOG(R)File 350:Derwent WPIX

010287755
WPI Acc No: 1995-189014/199525
XRAM Acc No: C95-087709
XRPX Acc No: N95-148307

Mfr. of **non-volatile semiconductor memory** - by forming polysilicon layer as source of solid phase diffusion and used as source line or bit line of low resistance

Patent Assignee: NKK CORP (NIKN)
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
JP 7106443	A	19950421	JP 93245331	A	19930930	199525	B

Priority Applications (No Type Date): JP 93245331 A 19930930
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
JP 7106443	A		8	H01L-021/8247	

Abstract (Basic): JP 7106443 A

The manufacturing method involves formation of polysilicon layers (15a, 15b) containing an impurity, on a **semiconductor substrate** (10). This polysilicon layer is used as the source of phase diffusion for forming the source and drain diffusion layers (17S, 17D) respectively.

A heat oxide film (18) is formed at the polysilicon layer. At the same time, a **tunnel** oxide **film** (18D) is formed between the frame and **drain** diffusion **regions.** A **floating gate** (19) is formed to cover both the heat oxide **film** and the **tunnel** oxide **film.**

ADVANTAGE - Provides high speed operation. Inhibits necessity to make two layers of **floating gate.** Enlarges **floating gate** and **capacitance** between **control gates** and sets up coupling ratio. Inhibits self alignment of source and drain diffusion layer formation. Obtains good electrical property as memory transistor. Inhibits poor contact and characteristics deterioration. Reduces leak current between polysilicon layer and **floating gate.**

Dwg.1/7

43/3,AB/7 (Item 7 from file: 350)
DIALOG(R)File 350:Derwent WPIX

009982998
WPI Acc No: 1994-250709/199431
XRAM Acc No: C94-114015
XRPX Acc No: N94-198131

Non-volatile semiconductor memory device - has ring-shaped channel region formed on **semiconductor substrate surface.** sepg. inner **drain region** from outer **source region**

Patent Assignee: MATSUSHITA ELECTRIC IND CO LTD (MATU); MATSUSHITA ELEC IND CO LTD (MATU); MATSUSHITA DENKI SANGYO KK (MATU)
Inventor: ICHIKAWA Y; NAKAO I; ODAKE Y; YASUSHI O; OKUDA Y
Number of Countries: 007 Number of Patents: 007
Patent Family:

```
Patent No     Kind   Date     Applicat No    Kind   Date      Week
EP 609829      A2  19940810  EP 94101463     A   19940201  199431  B
JP 6291290     A   19941018  JP 9410247      A   19940201  199501
EP 609829      A3  19950201  EP 94101463     A   19940201  199539
US 5510639     A   19960423  US 94189970     A   19940201  199622
                             US 95384791     A   19950209
EP 609829      B1  19971217  EP 94101463     A   19940201  199804
DE 69407318    E   19980129  DE 607318       A   19940201  199810
                             EP 94101463     A   19940201
KR 125113      B1  19971211  KR 941621       A   19940129  199951
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Priority Applications (No Type Date): JP 9315191 A 19930202
Patent Details:

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Patent No  Kind Lan Pg   Main IPC     Filing Notes
EP 609829     A2 E  20 H01L-029/788
   Designated States (Regional): DE FR GB NL
JP 6291290    A     13 H01L-027/115
US 5510639    A     16 H01L-029/788  Cont of application US 94189970
EP 609829     B1 E  24 H01L-029/788
   Designated States (Regional): DE FR GB NL
DE 69407318   E        H01L-029/788  Based on patent EP 609829
EP 609829     A3       H01L-029/788
KR 125113     B1       H01L-027/115
```

Abstract (Basic): EP 609829 A

Non-volatile semiconductor memory cell comprises a **semiconductor substrate** of a first conductivity type; a ring-shaped channel region of the first conductivity type formed on the top surface of the substrate; a **drain region** of a second conductivity type formed in a zone surrounded by the ring-shaped channel **region;** a **source region** of the second conductivity type formed outside the ring-shaped channel region; a first **gate insulation layer** formed on the top surface of the substrate covering the boundary between the ring-shaped channel **region** and the **drain region;** a ring-shaped **floating gate electrode** formed on the first **insulation layer;** a second **gate insulation layer** formed on the ring-shaped **floating gate electrode;** a **control gate electrode** which is **capacitive-coupled** with the ring-shaped **floating** gate **electrode** via the second **gate insulation layer,** and is electrically **insulated** from the substrate.

USE/ADVANTAGE - For fabrication of a **non-volatile memory** device. Electrical isolation between adjacent memory cell transistors is secured and the cells can be made extremely small and packaged in a high degree of integration; increased reading rate, and reduced deletion time.

1A,1B/11

Abstract (Equivalent): EP 609829 B

Non-volatile semiconductor memory cell comprises a **semiconductor substrate** of a first conductivity type; a ring-shaped channel region of the first conductivity type formed on the top surface of the substrate; a **drain region** of a second conductivity type formed in a zone surrounded by the ring-shaped channel **region;** a **source region** of the second conductivity type formed outside the ring-shaped channel region; a first **gate insulation layer** formed on the top surface of the substrate covering the boundary between the ring-shaped channel **region** and the **drain region;** a ring-shaped **floating gate electrode** formed on the first **insulation layer;** a second **gate insulation layer** formed on the ring-shaped **floating gate electrode;** a **control gate electrode** which is **capacitive-coupled** with the ring-shaped **floating** gate **electrode** via the second **gate insulation layer,** and is electrically **insulated** from the substrate.

USE/ADVANTAGE - For fabrication of a **non-volatile memory** device. Electrical isolation between adjacent memory cell transistors is secured and the cells can be made extremely small and packaged in a high degree of integration; increased reading rate, and reduced deletion time.

Dwg.1a/11

Abstract (Equivalent): US 5510639 A

A **non-volatile semiconductor memory** cell comprising: a **semiconductor substrate** of a first conductive type, the **semiconductor substrate** having a top surface; a ring-shaped channel region of the first conductive type embedded in the top **surface** of the **semiconductor substrate;** a **drain region** of a second conductive type formed in a zone surrounded by the ring-shaped channel region and embedded in the top **surface** of the **semiconductor substrate;** a **source region** of the second conductive type formed outside the ring-shaped channel region and embedded in the top **surface** of the **semiconductor substrate;** a first **gate insulation layer** formed on the top **surface** of the **semiconductor substrate** in such a manner as to cover the boundary between the ring-shaped channel **region** and the

drain region; a ring-shaped **floating gate electrode** formed from a conductive material on the first gate **insulation layer**; a second **gate insulation layer** formed on the ring-shaped **floating gate electrode**; and a **control gate electrode** which is **capacitive-coupled** with the ring-shaped **floating** gate **electrode** via the second **gate insulation layer**, and is electrically **insulated** from the **semiconductor substrate**.

Dwg.1b/11

43/3,AB/8 (Item 8 from file: 350)
DIALOG(R)File 350:Derwent WPIX

008881960
WPI Acc No: 1992-009229/199202
XRPX Acc No: N92-007100

Non-volatile semiconductor memory circuit - has substrate with drain and **control gate** of N-type conductivity and P-type emitter formed in surface with contact hole

Patent Assignee: TOSHIBA KK (TOKE)
Inventor: MATSUKAWA N; MIYAMOTO J
Number of Countries: 006 Number of Patents: 006
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
EP 463623	A	19920102	EP 91110653	A	19910627	199202	B
JP 4057369	A	19920225	JP 90166913	A	19900627	199222	
EP 463623	A3	19920812	EP 91110653	A	19910627	199336	
US 5350938	A	19940927	US 91721702	A	19910626	199438	
EP 463623	B1	19970319	EP 91110653	A	19910627	199716	
DE 69125212	E	19970424	DE 625212	A	19910627	199722	
			EP 91110653	A	19910627		

Priority Applications (No Type Date): JP 90166913 A 19900627
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 463623	A				
Designated States (Regional): DE FR GB IT					
JP 4057369	A		5	H01L-029/788	
US 5350938	A		12	H01L-029/68	
EP 463623	B1	E	13	H01L-027/115	
Designated States (Regional): DE FR GB IT					
DE 69125212	E			H01L-027/115	Based on patent EP 463623

Abstract (Basic): EP 463623 A

The memory cell includes a substrate (11) having an N type region (13) and a N type **drain region** (14) with a **control gate** (19). A P type emitter region (20) is formed in the surface **region** of the **drain region** (14) and an **insulating film** (21) overlies the **source region**, the **drain region**, emitter **region** and the **control gate**.

A contact hole (22) is formed in the **insulating film** so that the surface region of the emitter is exposed with an emitter electrode formed in the hole to constitute a PNP vertical bipolar transistor.

ADVANTAGE - Current driving **capacity** is improved for high speed. (13pp Dwg.No.1)

Abstract (Equivalent): EP 463623 B

A **nonvolatile semiconductor memory** device comprising: (1) a MOS transistor, comprising: (a) a semiconductor body (11) of a first conductivity type having a major surface and having first and second spaced regions (13, 14) containing an impurity of a second conductivity type opposite to said first conductivity type and having a surface; (b) a first **insulating layer** (16) on said major **surface** of said **semiconductor** body and extending at least between said first and second spaced regions; (c) a **floating gate** (17) on said first insulating **layer**; (d) a second **insulating layer** (18) on said-**floating gate**; and (e) a **control gate** (19) on said second **insulating layer**; and (II) a bipolar transistor, comprising: (a) an emitter region (24,25;25) of the first conductivity type, said emitter region being formed in a contact hole (22) etched in an **insulating film** (21) overlying said second spaced region (14), and on said surface of said second spaced region (14) and in contact therewith, said second spaced region comprising a base of said bipolar transistor, and said semiconductor body comprising a collector of said bipolar transistor; and (b) a collector contact region (12) comprising a buried region of the first conductivity type within said semiconductor body and spaced from said major surface thereof.

Dwg.1/10

Abstract (Equivalent): US 5350938 A

The memory cell transistor includes a **semiconductor substrate**, a N-type **source region**, a N-type **drain region**, a **control gate** and a P+-type emitter region, which is formed in the surface **region** of the **drain region**. An **insulating film** overlies the **source region**, the **drain region**, the emitter **region**, and the **control gate**.

A contact hole is formed in the **insulating film** so that the surface of the emitter region is exposed. An emitter electrode is formed in and around the contact hole. A PNP vertical bipolar transistor is constituted by the **semiconductor substrate** serving as a collector region, a P+-type buried layer serving as a collector contact, and the **drain region** serving as a base region.

ADVANTAGE - Data can be read out at high speed.

Dwg.9/10

43/3,AB/9   (Item 9 from file: 350)
DIALOG(R)File 350:Derwent WPIX

008411810
WPI Acc No: 1990-298811/199040
Related WPI Acc No: 1990-295208; 1990-295209
XRPX Acc No: N90-229832

Ferro-electric material for semiconductor memory - uses ferro-electric film sandwiched between diffuse layer and metal electrode

Patent Assignee: SEIKO EPSON CORP (SHIH); SEIKO EPSON CO LTD (SHIH)
Inventor: TAKENAKA K
Number of Countries: 004 Number of Patents: 008
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
EP 389762	A	19901003	EP 90102489	A	19900208	199040	B
JP 2232973	A	19900914	JP 8954222	A	19890307	199043	
JP 2304984	A	19901218	JP 89125804	A	19890519	199105	

JP 2304985	A	19901218	JP 89125805	A	19890519	199105
US 5099305	A	19920324				199215
EP 389762	B1	19950809	EP 90102489	A	19900208	199536
DE 69021419	E	19950914	DE 621419	A	19900208	199542
			EP 90102489	A	19900208	
KR 9500156	B1	19950110	KR 901323	A	19900205	199644

Priority Applications (No Type Date): JP 89125805 A 19890519; JP 8928940 A 19890208; JP 8928941 A 19890208; JP 8954222 A 19890307; JP 89125804 A 19890519

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 5099305	A		16		
EP 389762	B1	E	21	H01L-027/115	
DE 69021419	E			H01L-027/115	Based on patent EP 389762
KR 9500156	B1			H01L-029/788	

Abstract (Basic): EP 389762 A

The memory is formed by producing a ferroelectric substance film (107) formed on a diffused layer (103) which serves as a source or drain. An upper electrode (108) consists mainly of metal and the ferroelectric substance film is connected to the high-concentration diffused layer (103) at a contact hole (109).

A refactory metal silicide lower electrode may be formed on the high-concentration diffuse layer as a base for the ferroelectric film.

ADVANTAGE - Reduces number of manufacturing stages needed to form a **non-volatile memory** cell. (17pp Dwg.No.3/11)

Abstract (Equivalent): EP 389762 B

A semiconductor device comprising: a **semiconductor substrate** (101, 701), a high-concentration diffusion layer (103,703) formed on the substrate and being part of an active semiconductor element such as a MOS transistor, a ferroelectric substance film (107,708) sandwiched between an upper and a lower electrode (108, 709, 111, 114, 802, 1002), the lower electrode (111, 114, 802, 1002) being composed mainly of a metal and connected to the diffusion layer (103,703), characterized in that the lower electrode (111, 114, 1002) is formed on the diffusion layer (103,703) at an exposed contact portion thereof, the contact area between the ferroelectric substance film (107,708) and said lower electrode (111, 114, 1002) being smaller than that between said ferroelectric substance film (107, 708) and the upper electrode (108,709).

Dwg.5/11

Abstract (Equivalent): US 5099305 A

The ferroelectric memory device has a **semiconductor substrate** having a **surface** and an element forming region of a first conductivity type said substrate being provided with an **insulating layer** formed on the surface and constituting an isolating region surrounding the element forming region of said substrate. The substrate is also provided with at least one impurity diffused region layer of a second conductivity type opposite to the first conductivity type located in the element forming region and extending into the substrate from the surface. An MOS transistor is formed in the element forming region of the substrate and includesd a **source region** of the second conductivity type, a **drain region** of the second conductivity type, a **gate electrode** having a side wall, and a body of **insulating** material on the **gate electrode** side wall and contacting said substrate surface. One of the **drain region** and the **source region** is constituted by the at least one diffused region. A ferroelectric **capacitor** is formed on the substrate in the element forming region together with the transistor and has

capacitor electrodes and a ferroelectric film of PZT sandwiched between the **capacitor** electrodes. A portion of the diffused region layer is bordered, at the substrate surface, by the element isolating region and the body of insulating material. One of the **capacitor** electrodes has a metal layer of Pt formed directly on the diffused region portion. USE - As **non volatile memory** e.g. for computer system. (16pp)

43/3,AB/10 (Item 10 from file: 350)
DIALOG(R)File 350:Derwent WPIX

003970282
WPI Acc No: 1984-115826/198419
XRPX Acc No: N84-085624
Non-volatile semiconductor memory device - has timing circuit to ensure contents of non-selected memory cells do not change
Patent Assignee: TOKYO SHIBAURA DENKI KK (TOKE)
Inventor: WADA M
Number of Countries: 007 Number of Patents: 005
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
EP 107290	A	19840502	EP 83304916	A	19830825	198419	B
JP 59060797	A	19840406	JP 82171381	A	19820930	198420	
US 4571705	A	19860218	US 83527483	A	19830829	198610	
EP 107290	B	19891220				198951	
DE 3380998	G	19900125				199005	

Priority Applications (No Type Date): JP 82171381 A 19820930
Patent Details:
Patent No Kind Lan Pg Main IPC Filing Notes
EP 107290 A E 21
Designated States (Regional): DE FR GB IT NL
EP 107290 B E
Designated States (Regional): DE FR GB IT NL

Abstract (Basic): EP 107290 A

The memory device has electrically selectable, erasable and programmable functions and includes a matrix of memory cells each with a source and drain separately formed in a **semiconductor substrate**. A **floating gate** is formed on an **insulating film** formed on a channel **region** between the **source** and drain. A programme **electrode** opposes the **gate** and two **control gates** are formed in **capacitance-coupled** manner on an **insulation film** on the **floating gate**. Decoders are provided for properly selecting cells by setting a potential relation between the two **control gates**.

A timing circuit provides a programme inhibition period ranging over a period including a time point at which a programme potential for programming the contents in the cell selected by the decoders is supplied to the programme electrode. The timing circuit keeps one of the **control gates** of any cell at high potential during the inhibition period while keeping the other **control gate** at low potential. This ensures that the contents of the cells, other than the selected cell, do not charge.

8/11

Abstract (Equivalent): EP 107290 B

A **nonvolatile semiconductor memory** device with electrically selectable, erasable and programmable functions comprising:

a plurality of memory cells (11) arranged in a matrix array, each of said memory cells including a source (2) and a drain (3) separately formed in said

semiconductor substrate, a floating gate (5) formed on an **insulating film** (4a) formed on a channel **region** between said **source** and drain, a progam **electrode** (8) opposing said **floating gate** with a very thin

insulation film (4d) interposed therebetween, and first and second **control gates** (6,7) formed in a **capacitance-coupled** manner on an **insulation film** (4b,4c) formed on said **floating gate,** said memory cells on each of the columns of said matrix arrayed memory cells having said first **control gates** connected to one another, while said memory cells on each of the rows having said second **control gates** connected to one another; and select means (12,13,14) for properly selecting a predetermined memory cell by setting a potential relation between said first and second **control gates**, characterised in that there is provided timing means (15) for providing a program inhibition period (T) ranging over a period including a time point (t2) at which a program potential for programming the contents in the memory cell selected by said select means is supplied to each program electrode, said timing means keeping one of said first and second **control gates** of any memory cell at high

potential (H) during said program inhibition period, while keeping the other of said **control gates** at low potential (L), and that the program potential supplied to each program electrode in said matrix array is set during said program inhibition period, and that after said program inhibition period, the select means properly select a predetermined memory cell to allow the programming of data in said memory cell.

(13pp

Abstract (Equivalent): US 4571705 A

The device has a memory cell array including a MOSFET with a **floating gate** two **control gates** and a program **electrode**.

Column and row decoders are provided for selecting a specific memory cell as well as a program control circuit for programming data on the **floating gate.**

A timing circuit provides operation timings of the column and row decoders and the program control circuit.

The timing circuit sets up a program inhibit period ranging over time point at which a selected memory cell is to be erased and programmed.

In the program inhibit period, one of the **control gates** of each of the memory cells is at a high potential, while the other **control gate** is at low potential.

ADVANTAGE - Contents of memory cells other than those selected does not change when others are selectably erased or programmed.

(10pp

43/3,AB/11 (Item 1 from file: 347)
DIALOG(R)File 347:JAPIO
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07694407
NON-VOLATILE SEMICONDUCTOR MEMORY DEVICE AND MANUFACTURING METHOD THEREOF

PUB. NO.: 2003-188287 [JP 2003188287 A]
PUBLISHED: July 04, 2003 (20030704)
INVENTOR(s): MORI SEIICHI
ICHIGE MASAYUKI
TAKEUCHI YUJI
AIDA AKIRA
APPLICANT(s): TOSHIBA CORP
APPL. NO.: 2001-383894 [JP 2001383894]
FILED: December 18, 2001 (20011218)

ABSTRACT

PROBLEM TO BE SOLVED: To provide a **non-volatile semiconductor memory** device and the manufacturing method of the same, reduced in the affection of an interference due to a **coupling capacity** between neighbored memory cells and improved in the operational margin of the **memory** cell.
SOLUTION: The **non-volatile semiconductor memory** device is provided with a plurality of memory cell transistors 7, having a **gate** constituted of a **floating gate** 3 laminated on a **gate insulation film** 2 formed in an element region 16 on a p-type **semiconductor substrate** 1 through a **gate insulation film** 4 and a **control gate** 5, and an n-type diffusion layer 6 formed on the surface of the p-type **semiconductor substrate** 1 between the gates so as to become a source or a drain. Further, a source side selective transistor 9 is arranged on the source side of the memory cell transistor 7. A conductive layer 11 constituted of polysilicon added with impurities, for example, is embedded on the memory cell transistor 7 and the source side selective transistor 9 through an **insulation film** 10. In this case, the **source region** of the **source** side selective transistor 9 and the conductive layer 11 are directly connected.

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43/3,AB/12 (Item 2 from file: 347)
DIALOG(R)File 347:JAPIO
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07316390
NON-VOLATILE SEMICONDUCTOR STORAGE DEVICE AND MANUFACTURING METHOD THEREOF

PUB. NO.: 2002-184877 [JP 2002184877 A]
PUBLISHED: June 28, 2002 (20020628)
INVENTOR(s): FUJIWARA NOBUYO
ODANAKA SHINJI
FUJIMOTO HIROMASA
OGURA SEIKI
APPLICANT(s): MATSUSHITA ELECTRIC IND CO LTD
HALO LSI DESIGN & DEVICE TECHNOL INC
APPL. NO.: 2000-382233 [JP 2000382233]
FILED: December 15, 2000 (20001215)

ABSTRACT

PROBLEM TO BE SOLVED: To attain a high injection efficiency at a low

voltage, related to a **non-volatile semiconductor** storage device where a hot carrier is injected into a **floating gate electrode**.
SOLUTION: Related to a **semiconductor substrate** 11, an n-type **source region** 16 and an n-type **drain region** 17 are formed beside a **floating gate electrode** 13 and a **control gate electrode** 15 formed above it through a **capacity insulating film** 14. In the **drain region** 17, an n-type embedded drain 17a whose impurity concentration is lower than the **drain region** 17 is so formed that the end on the **source region** 16 side of the **drain region** 17 extends to the **source region** 16 side without reaching the **surface** of **semiconductor substrate** 11.

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43/3,AB/13 (Item 3 from file: 347)
DIALOG(R)File 347:JAPIO
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06883504
NON-VOLATILE MEMORY

PUB. NO.: 2001-111012 [JP 2001111012 A]
PUBLISHED: April 20, 2001 (20010420)
INVENTOR(s): FUJIMORI TAKAKAZU
APPLICANT(s): ROHM CO LTD
APPL. NO.: 11-291337 [JP 99291337]
FILED: October 13, 1999 (19991013)

ABSTRACT

PROBLEM TO BE SOLVED: To provide a **non-volatile memory** wherein a read-out margin is large, with a reliable read-out characteristics.

SOLUTION: Transistors of MFMIS structure are arrayed in matrix where a **floating gate** 4, ferroelectrics layer 5, and **control gate** 6 are sequentially laminated, through a **gate insulating film** 3, on the **surface** of a **semiconductor substrate** 1 between a **source** and **drain regions** formed on the **semiconductor substrate** . Here, the **control gate** is connected to a ward line, the **source region** is connected to a source line, and the **drain region** is connected to a drain line, while a floating line comprising a write-in gate so configured as to form a **capacitor** with the **floating gate** provided. The word line and the source line of the matrix in the same row are common-connected while the drain line and the floating line of the matrix in the same column are common-connected, with a source/drain voltage and a gate voltage allowed to be set independently.

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43/3,AB/14 (Item 4 from file: 347)
DIALOG(R)File 347:JAPIO
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06883409

SEMICONDUCTOR NON-VOLATILE MEMORY DEVICE AND **SEMICONDUCTOR** DEVICE

PUB. NO.: 2001-110917 [JP 2001110917 A]
PUBLISHED: April 20, 2001 (20010420)
INVENTOR(s): AOZASA HIROSHI
APPLICANT(s): SONY CORP
APPL. NO.: 11-282986 [JP 99282986]
FILED: October 04, 1999 (19991004)

ABSTRACT

PROBLEM TO BE SOLVED: To provide a **semiconductor non-volatile memory** device and a semiconductor device, where a **capacitive coupling** can be prevented from occurring between the **surface** of a **semiconductor substrate** and the side of a **gate electrode**, and cells can be lessened in area.

SOLUTION: A **semiconductor non-volatile memory** device is composed of a channel forming region formed in the active region of a **semiconductor substrate** 10, a **floating gate** formed on the channel forming region or a charge storage layer 21 such as a laminated **insulating film**, a **control gate** 31a formed on the charge storage layer 21, **source/drain regions** 11 formed inside the **semiconductor substrate** 10 as connected to the channel forming region, and a plate electrode 32 which is fixed at a certain potential such as a ground potential and formed on the active region on both the sides of the **control gate** 31a and the side wall of the **control gate** 31 through the intermediary of an **insulating film.**

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43/3,AB/15 (Item 5 from file: 347)
DIALOG(R)File 347:JAPIO
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06473110
NONVOLATILE MEMORY FOR HIGH LEVEL INTEGRATION AND ITS MANUFACTURE

PUB. NO.: 2000-058685 [JP 2000058685 A]
PUBLISHED: February 25, 2000 (20000225)
INVENTOR(s): CHOI JEONG-HYUK
APPLICANT(s): SAMSUNG ELECTRONICS CO LTD
APPL. NO.: 11-203289 [JP 99203289]
FILED: July 16, 1999 (19990716)
PRIORITY: 9829734 [KR 9829734], KR (Korea) Republic of, July 23, 1998 (19980723)

ABSTRACT

PROBLEM TO BE SOLVED: To increase **capacitance** at an **interlayer insulating film** , improve a coupling and lower the operation voltage, by arranging the **interlayer insulating film** surrounding the upper part and four side surfaces of a **floating gate**, and arranging a **control gate** surrounding the upper part and four side surfaces of the **interlayer insulating film**.

SOLUTION: **Source drain regions** 130, 132 of a second conductivity type are formed on a first conductivity type

semiconductor substrate. A first **insulating film** 106 is formed on a channel **region** formed between the **source drain regions** 130, 132, and a **floating gate** 108 is formed on the first insulating **film** 106. A second **interlayer insulating film** 124 is formed surrounding the upper part and four side surfaces in the direction of a word line and a bit line 142 of a **floating gate** 108. A **control gate** 154 is formed surrounding the upper part and four side surfaces of the second **interlayer insulating film** 124. As a result, **capacitance** at the second **interlayer insulating film** 124 is increased, a coupling ratio is improved, and an operating voltage of a **nonvolatile memory** element can be lowered.

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43/3,AB/16 (Item 6 from file: 347)
DIALOG(R)File 347:JAPIO
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04995691
NON-VOLATILE SEMICONDUCTOR MEMORY DEVICE

PUB. NO.: 07-288291 [JP 7288291 A]
PUBLISHED: October 31, 1995 (19951031)
INVENTOR(s): NIIMORI MASAHIRO
APPLICANT(s): NEC CORP [000423] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 06-104421 [JP 94104421]
FILED: April 19, 1994 (19940419)

ABSTRACT

PURPOSE: To improve cell transistor characteristics of a single-layered gate **non-volatile semiconductor memory** device.

CONSTITUTION: A silicon oxide layer 7 is formed on a **drain region** 3 and on a channel **region** between the **drain region** 3 and a **source region** 4 in a **semiconductor substrate** 1, and a silicon oxide layer 8 is formed on a programming region 6 in the **semiconductor substrate** 1. A **floating gate** 9 is formed on these silicon oxide **layers** 7, 8. The **capacitance** between the **floating gate** 9 and the programming region 6 is made smaller than the **capacitance** between the **floating gate** 9 and the **drain region** 3, so that F-N tunnel current is generated between the **floating gate** 9 and the programming region.

43/3,AB/17 (Item 7 from file: 347)
DIALOG(R)File 347:JAPIO
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04377574
NONVOLATILE MEMORY CELL

PUB. NO.: 06-021474 [JP 6021474 A]
PUBLISHED: January 28, 1994 (19940128)
INVENTOR(s): MOROOKA HISAO
SHINOHARA HISATO
IKEDA MASAAKI

TANAMURA YUUJI
NAGANO KATSUTO

APPLICANT(s):	TDK CORP [000306] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.:	03-335927 [JP 91335927]
FILED:	November 27, 1991 (19911127)
JOURNAL:	Section: E, Section No. 1541, Vol. 18, No. 225, Pg. 137, April 22, 1994 (19940422)

ABSTRACT

PURPOSE: To provide a greater **capacity nonvolatile memory** with a sufficient write/read speed.

CONSTITUTION: A memory cell comprises a storage electrode 2 formed on an insulating substrate 1, a ferrodielectric thin film 3 formed over the storage **electrode**, a **gate electrode** 4 formed on the ferrodielectric thin **film**, a **gate insulating film** 5 formed on the **gate electrode** 4, a semiconductor layer 6 formed on the **gate insulating film**, a **source region** 7 and a **drain region** both formed on a **semiconductor** layer **surface** , separated away from each other, and a source electrode 11 and a drain electrode 12 formed on the **source region** and the **drain region** respectively.

43/3,AB/18 (Item 8 from file: 347)
DIALOG(R)File 347:JAPIO
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04214772
NONVOLATILE SEMICONDUCTOR DEVICE AND ITS MANUFACTURE

PUB. NO.:	05-206472 [JP 5206472 A]
PUBLISHED:	August 13, 1993 (19930813)
INVENTOR(s):	KANAZAWA KENICHI
APPLICANT(s):	FUJITSU LTD [000522] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.:	04-012677 [JP 9212677]
FILED:	January 28, 1992 (19920128)
JOURNAL:	Section: E, Section No. 1465, Vol. 17, No. 640, Pg. 84, November 26, 1993 (19931126)

ABSTRACT

PURPOSE: To increase the **capacity** between an accumulating **electrode** and a **control electrode,** and prevent a drain turn-on current, and lessen malfunction by providing it with a plurality of conductive layers where accumulating electrodes are connected with each other, and providing it with a section where the **control electrode** arranged on the accumulating electrode extends between a plurality of conductive layers of the accumulating electrode.

CONSTITUTION: An accumulating electrode 5, which includes a lower-layer accumulating electrode 3 and a lower-layer accumulating electrode 4, is arranged through a **gate insulating film** 2 on the surface of a channel region 1 made of a **semiconductor substrate** or the like. Moreover, the lower-layer accumulating electrode 3 and the upper-layer electrode 4 are electrically connected with each other. A **control electrode** 9 not only covers the accumulating electrode 5 but also has a section 9a which extends between the upper-layer accumulating electrode 4 and the lower-layer accumulating electrode 3. Moreover, a **source region** 31 and a **drain region** 32

are arranged in opposition with a channel region between. Therefore, the opposite faces of the accumulating **electrode** 5 and the **control electrode** 9 become the three layers of the topside of the lower-layer accumulating electrode 3, the underside and the topside of the upper-layer accumulating electrode 4, and the area in opposition sharply improves.

43/3,AB/19 (Item 9 from file: 347)
DIALOG(R)File 347:JAPIO
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04063903
MANUFACTURE OF **SEMICONDUCTOR NONVOLATILE MEMORY**

PUB. NO.:	05-055603 [JP 5055603 A]
PUBLISHED:	March 05, 1993 (19930305)
INVENTOR(s):	NAKANISHI AKISHIGE
APPLICANT(s):	SEIKO INSTR INC [000232] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.:	03-217433 [JP 91217433]
FILED:	August 28, 1991 (19910828)
JOURNAL:	Section: E, Section No. 1394, Vol. 17, No. 356, Pg. 112, July 06, 1993 (19930706)

ABSTRACT

PURPOSE: To prevent stress from developing in a thin **gate insulating film** on a **semiconductor substrate** by performing ion implantation to dope the first thin film layer of polysilicon.

CONSTITUTION: A thin **gate insulating film** 12 is made on a **semiconductor substrate** 11 by thermal oxidation method. Next, polysilicon 13 at the first layer is formed by chemical vapor deposition, and it is patterned. And a **capacitor insulating film** 14 is made on this polysilicon 13 at the first layer. Polysilicon 15 at the second layer is made on this **capacitor insulating film** 14. Furthermore, the polysilicon 15 at the second layer is patterned by photolithography. And phosphorous is implanted into the polysilicon at the first layer and the vicinity of the **surface** of the **semiconductor substrate** 11 by ion implantation method, and is thermally diffused to form the doped polysilicon 13 at the first layer and an impurity diffused layer 16 at the same time. Then, a **source region** 17 and a **drain region** 18 are formed at the same time by ion implantation method.

43/3,AB/20 (Item 10 from file: 347)
DIALOG(R)File 347:JAPIO
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04063898
NONVOLATILE SEMICONDUCTOR MEMORY DEVICE AND ITS MANUFACTURE

PUB. NO.:	05-055598 [JP 5055598 A]
PUBLISHED:	March 05, 1993 (19930305)
INVENTOR(s):	KODAMA NORIAKI
APPLICANT(s):	NEC CORP [000423] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.:	03-212554 [JP 91212554]

FILED: August 26, 1991 (19910826)
JOURNAL: Section: E, Section No. 1394, Vol. 17, No. 356, Pg. 111, July 06, 1993 (19930706)

ABSTRACT

PURPOSE: To enable a sufficient **capacitance** between a **floating gate electrode** and a **control gate electrode** to be secured even if an element is miniaturized in a **nonvolatile semiconductor memory** device with the **floating gate electrode**.

CONSTITUTION: A title item is provided with a groove 6a reaching an inside of a **semiconductor substrate** 1 through a first **insulation film** 3 and a second **insulation film** 4 on an element region, a **source region** 9a and a **drain region** 10a separated by the groove 6a, and a **floating gate** 14a, a second **gate insulation film** 12a, and a **control gate electrode** 15a so that the groove 6a is covered including a surface of a first **gate insulation film** 7a formed on a surface of the groove 6a.

43/3,AB/21 (Item 11 from file: 347)
DIALOG(R)File 347:JAPIO
(c) 2004 JPO & JAPIO. All rts. reserv.

04045290
MANUFACTURING FOR **NON-VOLATILE MEMORY** DEVICE

PUB. NO.: 05-036990 [JP 5036990 A]
PUBLISHED: February 12, 1993 (19930212)
INVENTOR(s): NAKANISHI AKISHIGE
APPLICANT(s): SEIKO INSTR INC [000232] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 03-186498 [JP 91186498]
FILED: July 25, 1991 (19910725)
JOURNAL: Section: E, Section No. 1384, Vol. 17, No. 325, Pg. 145, June 21, 1993 (19930621)

ABSTRACT

PURPOSE: To prevent a leak current generated through a defect and provide high reliability in data-hold characteristics of a **semiconductor non-volatile memory**, by forming a tunnel **drain region** through an impurity that is thermally diffused in the horizontal direction in an ion implantation step.

CONSTITUTION: A thin **gate insulating film** 12 is formed on a semiconductor device 11. First layered polysilicon 13 is formed as a **floating gate electrode** and is patterned, and a **capacitive insulating film** 14 is formed thereon. On the **capacitive insulating film** 14, secondary polysilicon 15 is formed as a **control gate electrode** and is patterned. Then, in an ion-implantation step, phosphorus is implanted to a surface area near a **drain region** in the **semiconductor substrate** 11 so as to diffuse implanted ions in a-horizontal direction and form a tunnel **drain region** 16. Lastly, arsenic is implanted to a surface area in the substrate 11 so as to form a **source region** 17 and a **drain region** 18.

43/3,AB/22 (Item 12 from file: 347)

DIALOG(R)File 347:JAPIO
(c) 2004 JPO & JAPIO. All rts. reserv.

03439978
ELECTRICALLY ERASABLE **NONVOLATILE SEMICONDUCTOR MEMORY**

PUB. NO.: 03-102878 [JP 3102878 A]
PUBLISHED: April 30, 1991 (19910430)
INVENTOR(s): KOJIMA YOSHIKAZU
APPLICANT(s): SEIKO INSTR INC [000232] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 01-241013 [JP 89241013]
FILED: September 18, 1989 (19890918)
JOURNAL: Section: E, Section No. 1093, Vol. 15, No. 291, Pg. 67, July 24, 1991 (19910724)

ABSTRACT

PURPOSE: To prevent the miswriting into a memory after erasion by providing an erasion voltage lowering doping area at the **surface** of the **semiconductor substrate** between a **source region** and a **drain region**.

CONSTITUTION: The doping area 8 to lower erasion voltage, which includes donor impurities, is formed at the surface of a P-type silicon substrate 1, and thereon a **floating** gate **electrode** 5, a **control gate insulating film** 6, and a **control gate electrode** 7 are formed through a **gate insulating film** 4. Furthermore, an N-type **source region** 2 and a **drain region** 3 are formed on the surface of the substrate 1 with the **floating gate electrode** 5 as a mask in self alignment. Hereupon, the **control gate electrode** 7 is **coupled** strongly in **capacity** with the **floating** gate **electrode** 5 through the **control gate insulating film** 6, and by applying voltage to the **control gate electrode** 7, the potential of the **floating gate** 5 is **controlled** indirectly. Since an erasion voltage lowering doping area 8 is provided, as the result that the erasion voltage can be lowered and that the breakdown strength between the erasion area and the substrate can be elevated, miswriting can be prevented.

```
   23jun04 14:16:38 User267149 Session D1469.1

File 342:Derwent Patents Citation Indx 1978-04/200436
       (c) 2004 Thomson Derwent

? S PN=(US 6545312 OR US 6642572)
? MAP PN/CT=
? MAP PN/CG=

Set      Items   Description
S1          15   S1:S3
S2           8   S1 AND (NON()VOLATIL? OR NONVOLATIL?)(3N)(SEMICONDUCT? OR -
             MEMOR?)
S3           8   IDPAT (sorted in duplicate/non-duplicate order)
S4           4   IDPAT (primary/non-duplicate records only)
S5           7   S1 NOT S2
S6           7   IDPAT (sorted in duplicate/non-duplicate order)
S7           5   IDPAT (primary/non-duplicate records only)
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4/3,AB/1     (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX
(c) 2004  Thomson Derwent. All rts. reserv.

013786159
WPI Acc No: 2001-270370/200128
XRPX Acc No: N01-194002
  Split-gate type non-volatile semiconductor memory
  , has extension section of drain area formed near floating gate
  electrode, whose impurity concentration is almost equal to main portion
  of drain
Patent Assignee: HALO LSI DESIGN & DEVICE TECHNOLOGY INC (HALO-N);
  MATSUSHITA DENKI SANGYO KK (MATU  )
Number of Countries: 001  Number of Patents: 001
Patent Family:
Patent No      Kind   Date     Applicat No    Kind   Date      Week
JP 2001057394  A    20010227  JP 99242985     A   19990830  200128  B

Priority Applications (No Type Date): JP 99161929 A 19990609
Patent Details:
Patent No  Kind Lan Pg   Main IPC    Filing Notes
JP 2001057394 A     26 H01L-021/8247

Abstract (Basic): JP 2001057394 A
Abstract (Basic):
        NOVELTY - Insulating films (12,14) are formed on conductive area of
    substrate (10) and one side along gate length of control gate electrode
    (13). N-type drain and source (17,18) are formed respectively on
    adjacent-opposite areas of floating gate electrode (16) capacitively
    coupled to electrode (13). Impurity concentration of extension section
    (17a) of electrode (16) of drain is same as that of main portion (17b).
        DETAILED DESCRIPTION - The control gate electrode is formed on the
    insulating film (12). An INDEPENDENT CLAIM is also included for
    non-volatile semiconductor memory.
        USE - Split-gate type non-volatile semiconductor
    memory for e.g. flash type EEPROM.
        ADVANTAGE - By forming the drain area directly below the floating
    gate electrode, increase in write-in velocity, reduction of write-in
    voltage are achieved, thereby improving write-in efficiency.
        DESCRIPTION OF DRAWING(S) - The figure shows the top and sectional
    views of non-volatile semiconductor memory.
        Semiconductor substrate (10)
        Insulating films (12,14)
        Control gate electrode (13)
        Floating gate electrode (16)
        N-type drain (17)
        Extension section (17a)
        Main portion (17b)
        N-type source (18)
        pp; 26 DwgNo 1/21


 4/3,AB/2     (Item 2 from file: 350)
DIALOG(R)File 350:Derwent WPIX
(c) 2004  Thomson Derwent. All rts. reserv.

012615625
WPI Acc No: 1999-421729/199936
XRPX Acc No: N99-315163
  Nonvolatile semiconductor memory used in VLSI and
```

portable devices with increased speed and efficiency

Patent Assignee: HALO LSI DESIGN & DEVICE TECHNOLOGY INC (HALO-N); MATSUSHITA ELECTRIC IND CO LTD (MATU); MATSUSHITA DENKI SANGYO KK (MATU)

Inventor: AKAMATSU K; HORI A; KATO J; ODANAKA S; OGURA S

Number of Countries: 027 Number of Patents: 007

Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
EP 935293	A2	19990811	EP 99100645	A	19990114	199936	B
JP 11260944	A	19990924	JP 996656	A	19990113	199951	
JP 2982901	B2	19991129	JP 996656	A	19990113	200002	
US 6051860	A	20000418	US 988572	A	19980116	200026	
US 6184553	B1	20010206	US 988572	A	19980116	200109	
			US 99325772	A	19990604		
US 20010001295	A1	20010517	US 988572	A	19980116	200128	
			US 99325772	A	19990604		
			US 2000727536	A	20001204		
US 6358799	B2	20020319	US 988572	A	19980116	200224	
			US 99325772	A	19990604		
			US 2000727536	A	20001204		

Priority Applications (No Type Date): US 988572 A 19980116; US 99325772 A 19990604; US 2000727536 A 20001204

Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 935293	A2	E	50	H01L-029/788	
Designated States (Regional): AL AT BE CH CY DE DK ES FI FR GB GR IE IT LI LT LU LV MC MK NL PT RO SE SI					
JP 11260944	A		32	H01L-021/8247	
JP 2982901	B2		28	H01L-021/8247	Previous Publ. patent JP 11260944
US 6051860	A			H01L-029/72	
US 6184553	B1			H01L-027/115	Cont of application US 988572 Cont of patent US 6051860
US 20010001295	A1			H01L-021/336	Cont of application US 988572 Div ex application US 99325772
US 6358799	B2			H01L-021/336	Cont of application US 988572 Div ex application US 99325772 Cont of patent US 6051860 Div ex patent US 6184553

Abstract (Basic): **EP 935293** A2

Abstract (Basic):

NOVELTY - A p-type silicon substrate (1) with first (upper) surface (11) linked to second surface (12) by 50 nm step (13) has 3.3 V, 0 V, and 5.5 V applied to control gate (6), source region (7) and drain region (8) respectively, while hot electrons generated in channel region (9) are injected into floating gate (4) to write data. In reading, the voltages between the source region and drain region are reversed.

DETAILED DESCRIPTION - N-type source region and p-type channel region are formed on first upper surface. N-type drain region is formed on second lower surface. Source, drain and channel regions are each subdivided into regions of high and low impurity concentration. Step region may be inclined or curved. Control gate and floating gate are capacitive coupled by insulating film. An independent claim is included for method for fabricating **nonvolatile semiconductor memory** device.

USE - VLSI memory devices. Portable units.

ADVANTAGE - High speed write and low power consumption operation. Increased electron injection efficiency. Lateral electric fields under control gate and floating gate are increased. Improved data erasure characteristics.

DESCRIPTION OF DRAWING(S) - The drawing shows structure of semiconductor device.

Substrate (1)
floating gate (4)
control gate (6)
source region (7)
drain region (8)
channel region (9)
first (upper) surface region (11)
second (lower) surface region (12)
step region (13)
pp; 50 DwgNo 1A/30

4/3,AB/3 (Item 3 from file: 350)
DIALOG(R)File 350:Derwent WPIX

010792263
WPI Acc No: 1996-289216/**199630**
XRAM Acc No: C96-092574
XRPX Acc No: N96-242706

High reliability **non-volatile memory** and methods of mfr. - has floating gate formed above inclined part of channel, with source formed at higher level than drain, for improved device durability

Patent Assignee: SHARP KK (SHAF)
Inventor: MATSUSHITA T
Number of Countries: 005 Number of Patents: 006
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
EP 718895	A2	19960626	EP 95302992	A	19950502	199630	B
JP 8227944	A	19960903	JP 95107477	A	19950501	199645	
EP 718895	A3	19970326	EP 95302992	A	19950502	199728	
EP 718895	B1	20000927	EP 95302992	A	19950502	200048	
DE 69518970	E	20001102	DE 618970	A	19950502	200062	
			EP 95302992	A	19950502		
JP 2002151609	A	20020524	JP 95107477	A	19950501	200250	
			JP 2001290442	A	19950501		

Priority Applications (No Type Date): JP 94317107 A 19941220
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 718895	A2	E	53	H01L-029/788	
Designated States (Regional): DE FR GB NL					
JP 8227944	A		26	H01L-021/8247	
EP 718895	A3			H01L-029/788	
EP 718895	B1	E		H01L-029/788	
Designated States (Regional): DE FR GB NL					
DE 69518970	E			H01L-029/788	Based on patent EP 718895
JP 2002151609	A		27	H01L-021/8247	Div ex application JP 95107477

Abstract (Basic): EP 718895 A

Non-volatile memory has: substrate of first conductivity type, source (10) and drain (11) of second conductivity type, channel (4) at least partially overlapping gate insulation (5), floating gate (7), interlayer insulation (8) and control gate (9). The source and drain regions are formed with a constant depth in the substrate surface and at least part of either is formed in a surface having a crystal face orientation different from the main surface of the substrate. The channel contacts the drain and has an inclined region the surface of which has a crystal orientation different from the main surface of the substrate. The source region is placed relatively higher than the drain region. Also claimed is a TFT having a similar structure. Further claimed are methods for forming the **non-volatile memory** are claimed.

ADVANTAGE - Reliability and durability of the oxide film below the floating gate is improved so that device performance is improved. Punch-through is eliminated, write-erase speed is high and erroneous erasure is prevented.

Dwg.1/46

4/3,AB/4 (Item 4 from file: 350)
DIALOG(R)File 350:Derwent WPIX

008734225
WPI Acc No: 1991-238241/**199132**
Related WPI Acc No: 1991-215366; 1992-382360; 1993-295237
XRAM Acc No: C91-103637
XRPX Acc No: N91-181693

Non-volatile electrically alterable **semiconductor** **memory** device - having single transistor for each cell and recrystallised floating gate

Patent Assignee: SILICON STORAGE TECHNOLOGY INC (SILI-N); SILICON STORAGE TEC (SILI-N)
Inventor: JENG C; YEH B; JENQ C S; JENQ C
Number of Countries: 017 Number of Patents: 010
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
WO 9111026	A	19910725				199132	B
US 5045488	A	19910903	US 90468003	A	19900122	199138	
US 5067108	A	19911119	US 90467918	A	19900122	199149	
EP 464196	A	19920108	EP 91904033	A	19910118	199202	
US 5202850	A	19930413	US 90467918	A	19900122	199317	
			US 91748627	A	19910821		
US 5278087	A	19940111	US 90467918	A	19900122	199403	
			US 91748627	A	19910821		
			US 92961256	A	19921015		
EP 464196	A4	19930818	EP 91904033	A		199527	
CA 2051686	C	20011023	CA 2051686	A	19910118	200170	
			WO 91US433	A	19910118		
EP 464196	B1	20020508	EP 91904033	A	19910118	200231	
			WO 91US433	A	19910118		
DE 69133003	E	20020613	DE 633003	A	19910118	200246	
			EP 91904033	A	19910118		
			WO 91US433	A	19910118		

Priority Applications (No Type Date): US 90468003 A 19900122; US 90467907 A 19900122; US 90467918 A 19900122; US 91748627 A 19910821; US 92961256 A 19921015
Patent Details:
Patent No Kind Lan Pg Main IPC Filing Notes
WO 9111026 A
Designated States (National): CA JP
Designated States (Regional): BE CH DE DK ES FR GB GR IT LI LU NL SE
EP 464196 A
Designated States (Regional): AT BE CH DE ES FR GB GR IT LI LU NL SE
US 5202850 A 15 G11C-011/40 Div ex application US 90467918

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                                           Div ex patent US 5067108
US 5278087    A     16 H01L-021/266  Div ex application US 90467918
                                           Div ex application US 91748627
                                           Div ex patent US 5067108
                                           Div ex patent US 5202850
CA 2051686    C  E     H01L-027/02   Based on patent WO 9111026
EP 464196     B1 E     H01L-027/02   Based on patent WO 9111026
   Designated States (Regional): AT BE CH DE DK ES FR GB GR IT LI LU NL SE
DE 69133003   E        H01L-027/02   Based on patent EP 464196
                                           Based on patent WO 9111026
```

Abstract (Basic): WO 9111026 A

An electrically programmable and erasable memory device (10) has a number of storage sites, a number of row address lines, a number of column address lines and a common line. Each combination of a particular row address line and a particular column address line defines a different one of the storage sites.

Each storage site consists of a single transistor which comprises: (a) a source (16) coupled to the common line; (b) a drain (14) coupled to one of the column address lines; (c) a control gate (29) coupled to one of the row address lines; (d) a floating gate (22) between the control gate, the source, and the drain and being capacitively coupled to the drain; (e) means for injecting hot electrons generated by abrupt potential drop onto the floating gate when the corresponding column and row address lines are raised at a first selected potential above that of the common line, with the potential applied to the column address line being above that applied to the row address line; and (f) a means for inducing Fowler-Nordheim tunnelling of charges from floating gate to control gate when the corresponding row address line is raised to a second selected potential above the associated column address line.

USE/ADVANTAGE - Used for **non-volatile** electrically alterable **semiconductor memory** devices. Obviates problems found with prior art devices due to poor reliability and manufacturability of thin oxide tunnel layers and allow redn. in size. (49pp Dwg.No.1/4)

Abstract (Equivalent): US 5278087 A

Charges to and from an isolated gate through a tunnelling dielectric material are transported using a charge injection semiconductor gate, in a semiconductor integrated circuit device, formed by (A) depositing a layer of poly-Si or amorphous Si on a substrate, (b) covering this layer with a protective material (PM) and annealing the layer to form recrystallised Si (RS), (C) defining a charge injection region along a RS edge in the layer and rendering the layer conducting and (D) growing the tunnelling dielectric material on the layer and forming the isolated gate on the dielectric material.

The charge injection region is defined by (a) selectively etching a portion of the PM to expose RS, (b) oxidising the exposed RS to form a layer of SiO2 having the charge injection region along the border of the SiO2 and PM, (c) removing the PM to expose other portions of the RS and (d) anisotropically etching the other portions of the RS.

USE/ADVANTAGE - Used as single transistor electrically programmeable and erasable memory device. The device can be readily produced.

Dwg.1/4

US 5202850 A

Single transistor **non-volatile** electrically alterable **semiconductor memory** cell (10) comprises a Si substrate (12), e.g. of P type, within which source (16) and drain (18) regions are defined, with a channel region (18) in between. Over these regions is a layer (20) of insulating material and a floating gate (22) which

is positioned over part of the channel region and part of the drain region. The gate is pref. a recrystallised poly-Si gate. A second insulating layer (28) is partially over the floating gate and a control gate (29) has a portion (28) over the second layer and a second portion (30) over the first layer and adjacent to the side wall (26) of the second layer.

ADVANTAGE - Ease of mfr., good yield.

Dwg.2/4

US 5067108 A

Electrically programmable and erasable memory device has a substrate of first-conductivity type semiconductor material. First and second spaced-apart regions defined in the substrate are of second-conductivity type with a channel region. An electrically conductive recrystallised floating gate is disposed over a first insulating layer and extends over a portion of the channel region and second region. A second insulating layer is disposed over and immediately adjacent the floating gate and is thick enough to permit Fouler-Nordheim tunnelling of charges. This occurs from floating gate to control gate when the selected row line is raised to a second predetermined potential above the selected column line.

ADVANTAGE - Memory device has recrystallised floating gate. (15pp)

US 5045488 A

Producing electrically programmable and erasable memory device comprises (a) defining the substrate; (b) growing layer of dielectric material over the substrate; (c) depositing layer of polysilicon over dielectric material, (d) covering polysilicon with protective layer; (e) patterning and exposing isolation region in protective layer with masking material to form exposed isolation region; (f) removing protective and polysilicon layers leaving stack at sidewalls; (g) removing masking; (h) depositing second protective then polysilicon layers; (i) removing 2nd polysilicon layer except around stack sidewalls; (j) converting polysilicon adjacent stack into silicon oxide spacer; (k) implanting channel stop implant everywhere except protected spacer; (l) removing spacer; (m) thermally growing field oxide adjacent stack and (n) removing 1st protective and polysilicon layers.

USE - To produce single transistor, **non-volatile**, electrically alterable **semiconductor memory** device. (15pp)

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7/3,AB/1     (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX
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014657469
WPI Acc No: 2002-478173/200251
Related WPI Acc No: 2000-610782
XRAM Acc No: C02-135997
XRPX Acc No: N02-377530
  Split gate flash memory cells fabrication method involves forming control
  gate on floating gate, which are separated by polyoxide and nitride
  spacer
Patent Assignee: WINBOND ELECTRONICS CORP (WINB-N)
Inventor: LEU L
Number of Countries: 001  Number of Patents: 001
Patent Family:
Patent No     Kind   Date    Applicat No    Kind   Date      Week
US 6365459     B1  20020402  US 98156583     A   19980918  200251  B
                             US 2000528516   A   20000320

Priority Applications (No Type Date): US 98156583 A 19980918; US 2000528516
  A 20000320
Patent Details:
Patent No  Kind Lan Pg   Main IPC    Filing Notes
US 6365459    B1     9 H01L-021/8247 Div ex application US 98156583
                                     Div ex patent US 6114723

Abstract (Basic): US 6365459 B1
Abstract (Basic):
        NOVELTY - A floating gate with an overlaying polyoxide layer (16)
    is formed on a substrate. A chemical vapor deposition (CVD) nitride
    side wall spacer is formed around the floating gate by CVD nitride
    deposition followed by anisotropic etching of CVD nitride film. A
    control gate which is formed on the floating gate, are separated by the
    polyoxide and nitride spacer. A source (17) and drain (18) are formed
    in the substrate using source and drain implantation.
        USE - For fabrication of split gate flash memory.
        ADVANTAGE - Size of the floating gate and overall memory cell
    dimension are made smaller. Allows scaling of flash memory cells to be
    achieved without incurring large expenses.
        DESCRIPTION OF DRAWING(S) - The figure shows a side view of flash
    memory cell after drain implantation.
        Polyoxide layer (16)
        Source (17)
        Drain (18)
        pp; 9 DwgNo 3E/3


 7/3,AB/2     (Item 2 from file: 350)
DIALOG(R)File 350:Derwent WPIX
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014446449
WPI Acc No: 2002-267152/200231
XRPX Acc No: N02-207684
  Semiconductor device e.g. DRAM has depletion layer that is formed in
  floating gate electrode near insulating film such that no voltage is
  applied between electrode and substrate
Patent Assignee: FUJITSU LTD (FUIT  )
Inventor: HORIGUCHI N; USUKI T
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Number of Countries: 002 Number of Patents: 003

Patent Family:

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Patent No       Kind   Date      Applicat No     Kind   Date      Week
US 20020003255  A1   20020110  US 2001814000    A    20010322  200231  B
JP 2002016155   A    20020118  JP 2000198390    A    20000630  200231
US 6462374      B2   20021008  US 2001814000    A    20010322  200269
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Priority Applications (No Type Date): JP 2000198390 A 20000630

Patent Details:

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Patent No  Kind Lan Pg   Main IPC     Filing Notes
US 20020003255 A1    27 H01L-029/788
JP 2002016155 A      14 H01L-021/8247
US 6462374    B2        H01L-029/788
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Abstract (Basic): US 20020003255 A1

Abstract (Basic):

NOVELTY - An insulation film (14) is formed between a semiconductor substrate (10) and a floating gate electrode (22). An insulation film (24) is formed between the gate electrode and a control gate electrode (26). A depletion layer is formed in the gate electrode (22) near the film (14) such that no voltage is applied between the gate electrode (22) and the substrate.

DETAILED DESCRIPTION - An INDEPENDENT CLAIM is also included for semiconductor device fabrication method.

USE - E.g. dynamic random access memory (DRAM).

ADVANTAGE - The floating gate electrode retains information for long period of time.

DESCRIPTION OF DRAWING(S) - The figure shows a sectional view of the semiconductor device.

Semiconductor substrate (10)
Insulation films (14,24)
Floating gate electrode (22)
Control gate electrode (26)
pp; 27 DwgNo 1/18

7/3,AB/3   (Item 3 from file: 350)
DIALOG(R)File 350:Derwent WPIX

013749416
WPI Acc No: 2001-233645/**200124**
Related WPI Acc No: 2001-210589
XRPX Acc No: N01-166875

New poly spacer split gate cell with extremely small cell size - where the self-aligned nature of the second gate to the first gate allows a very small dual-gate cell to be formed

Patent Assignee: MOSEL VITELIC INC (MOSE-N); SUNG K (SUNG-I)
Inventor: SUNG K
Number of Countries: 002 Number of Patents: 004

Patent Family:

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Patent No       Kind   Date      Applicat No     Kind   Date      Week
TW 409416        A   20001021  TW 99101336      A    19990128  200124  B
US 6242774       B1  20010605  US 9893841       A    19980519  200139  N
                               US 99266285      A    19990311
US 20010011744  A1   20010809  US 9893841       A    19980519  200147
                               US 99266285      A    19990311
                               US 2001822563    A    20010330
US 6440796       B2  20020827  US 9893841       A    19980519  200259  N
                               US 99266285      A    19990311
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                              US 2001822563   A   20010330

Priority Applications (No Type Date): TW 99101336 A 19990128; US 99266285 A
  19990311
Patent Details:
Patent No  Kind Lan Pg   Main IPC     Filing Notes
TW 409416     A        H01L-027/115
US 6242774    B1       H01L-029/788  CIP of application US 9893841
US 20010011744 A1       H01L-029/76   CIP of application US 9893841
                                     Div ex application US 99266285
                                     CIP of patent US 6194272
                                     Div ex patent US 6242774
US 6440796    B2       H01L-021/336  CIP of application US 9893841
                                     Div ex application US 99266285
                                     CIP of patent US 6194272
                                     Div ex patent US 6242774

Abstract (Basic): TW 409416 A
Abstract (Basic):
        NOVELTY - A dual-gate cell structure with self-aligned gates. A
    polysilicon spacer forms a second gate (213) separated from a first
    gate (201), which is also polysilicon, by a dielectric layer (207). A
    drain region (219) and a source region (221) are formed next to the
    gates within a floating well. In one embodiment, the second gate (213)
    acts as a floating gate in a flash cell. The floating gate may be
    programmed and erased by the application of appropriate voltage levels
    to the first gate (201), source (221), and/or drain (219). The
    self-aligned nature of the second gate (213) to the first gate (201)
    allows a very small dual-gate cell to be formed.
         DwgNo 0/0


 7/3,AB/4     (Item 4 from file: 350)
DIALOG(R)File 350:Derwent WPIX
(c) 2004  Thomson Derwent. All rts. reserv.

008711345
WPI Acc No: 1991-215366/199129
Related WPI Acc No: 1991-238241; 1992-382360; 1993-295237
XRPX Acc No: N91-164383
  Single transistor electrically programmable and erasable memory cell -
  includes source, drain and channel region on substrate, insulating
  layers, floating gate and control gate
Patent Assignee: SILICON STORAGE TECHNOLOGY INC (SILI-N); SILICON STORAGE
  TEC (SILI-N)
Inventor: YEH B
Number of Countries: 002  Number of Patents: 002
Patent Family:
Patent No      Kind   Date     Applicat No     Kind   Date     Week
US 5029130      A    19910702  US 90467907      A   19900122  199129  B
DE 69133003     E    20020613  DE 633003        A   19910118  200246
                               EP 91904033      A   19910118
                               WO 91US433       A   19910118

Priority Applications (No Type Date): US 90467907 A 19900122; US 90467918 A
  19900122; US 90468003 A 19900122
Patent Details:
Patent No  Kind Lan Pg   Main IPC     Filing Notes
DE 69133003   E        H01L-027/02   Based on patent EP 464196
                                     Based on patent WO 9111026
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Abstract (Basic): US 5029130 A

The single transistor has a source, a drain with a channel region defined on a substrate. A first insulating layer is over the source, channel and drain regions. A floating gate is positioned on top of the first insulating layer over a portion of the channel region and over a portion of the drain region. A second insulating layer has a top wall which is over the floating gate. A control gate has a first portion which is over the first insulating layer and immediately adjacent to the side wall of the second insulating layer. The control gate has a second portion which is over the top wall of the second insulating layer and is over the floating gate.

Erasure of the cell is accomplished by the mechanism of Fowler-Nordheim tunneling from the floating gate through the second insulating layer to the control gate. Programming is accomplished by electrons from the source migrating through the channel region underneath the control gate and they by abrupt potential drop injecting through the first insulating layer into the floating gate.

ADVANTAGE - Improved reliability. (15pp Dwg.No.1/4)

7/3,AB/5   (Item 5 from file: 350)
DIALOG(R)File 350:Derwent WPIX

008585925
WPI Acc No: 1991-089957/**199113**
XRAM Acc No: C91-038413
XRPX Acc No: N91-069345

Sensitive recording material - has photosensitive layer on support contg. silver halide, polymerisable cpd., initiator and reducing agent

Patent Assignee: FUJI PHOTO FILM CO LTD (FUJF)
Number of Countries: 001 Number of Patents: 001
Patent Family:

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Patent No     Kind   Date     Applicat No    Kind   Date      Week
JP 3033748     A   19910214  JP 89167970     A   19890629  199113  B
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Priority Applications (No Type Date): JP 89167970 A 19890629

Abstract (Basic): JP 3033748 A

The recording material has a photosensitive layer on a support, contg. at least a photosensitive silver halide; a polymerisable cpd.; a thermopolymerisation or photopolymerisation initiator; and a reducing agent of formula (I) or (II). In the formulae R1 = H, alkyl, aryl, heterocyclic gp.; R2-R6 = H, halo, alkyl, aryl, heterocyclic gp., acyl, acyloxy, COOH, H2HCO, alkoxy-carbonyl, aryloxycarbonyl, CN, alkoxy, aryloxy, sulfonyl, H2NSO2, sulfenyl, sulphinyl, NH2, acylamino, alkoxycarbonylamino, H2NCONH, HO3SNH, H2NSO2NH; two of R2-R6 may form a ring; cpd. (I) or (II) may form a polymer.

Recording method comprises image-wise exposing the recording material and simultaneously or after exposure, heating the recording material or irradiating uniformly the recording material with light after heating to polymerise the polymerisable cpd. in the exposed part to form a polymer image.

USE/ADVANTAGE - The recording material has a good sensitivity, and can form a polymer image by rapid treatment by dry process or by use of little water.

Dwg.0/0

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     (FILE 'HOME' ENTERED AT 15:27:38 ON 23 JUN 2004)

     FILE 'WPIX, INPADOC, JAPIO, PATOSEP, PATOSWO' ENTERED AT 15:29:10 ON 23
     JUN 2004
                E JP2000-200579/AP,PRN
L1            9 S E4
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L1   ANSWER 1 OF 9  WPIX COPYRIGHT 2004 THOMSON DERWENT on STN
AN   2002-331812 [37]   WPIX
DNN  N2002-260534
TI   Non-volatile semiconductor memory e.g. split/stacked gate flash EEPROM,
     has protective insulating film on side surfaces of control gate electrode
     formed in substrate with gate oxide film.
DC   U11 U12 U13 U14
IN   FUJIMOTO, H; KAMADA, A; KUSUMI, M; NORO, F; ODANAKA, S; OGURA, S
PA   (HALO-N) HALO LSI DESIGN & DEVICE TECHNOLOGY INC; (MATU) MATSUSHITA
     ELECTRIC IND CO LTD; (MATU) MATSUSHITA DENKI SANGYO KK; (FUJI-I) FUJIMOTO
     H; (KAMA-I) KAMADA A; (KUSU-I) KUSUMI M; (NORO-I) NORO F; (ODAN-I) ODANAKA
     S; (OGUR-I) OGURA S
CYC  30
PI   EP 1172856       A1 20020116 (200237)* EN  105    H01L027-115
         R: AL AT BE CH CY DE DK ES FI FR GB GR IE IT LI LT LU LV MC MK NL PT
            RO SE SI TR
     JP 2002083886    A  20020322 (200237)       58    H01L021-8247
     US 2002039822    A1 20020404 (200237)             H01L021-336
     KR 2002004857    A  20020116 (200249)             H01L029-788
     US 6545312       B2 20030408 (200327)             H01L029-788
     TW 501284        A  20020901 (200334)             H01L029-788
     US 2003141540    A1 20030731 (200354)             H01L029-76
     US 2003173616    A1 20030918 (200362)             H01L029-788
     US 6642572       B2 20031104 (200374)             H01L029-788
     US 2004071024    A1 20040415 (200426)             G11C007-00
ADT  EP 1172856 A1 EP 2001-116049 20010702; JP 2002083886 A JP 2001-150649
     20010521; US 2002039822 A1 US 2001-897417 20010703; KR 2002004857 A KR
     2001-39516 20010703; US 6545312 B2 US 2001-897417 20010703; TW 501284 A TW
     2001-116264 20010703; US 2003141540 A1 Div ex US 2001-897417 20010703, US
     2003-382520 20030307; US 2003173616 A1 Div ex US 2001-897417 20010703, US
     2003-382508 20030307; US 6642572 B2 Div ex US 2001-897417 20010703, US
     2003-382520 20030307; US 2004071024 A1 Div ex US 2001-897417 20010703, Div
     ex US 2003-382520 20030307, US 2003-679431 20031007
FDT  US 2003141540 A1 Div ex US 6545312; US 2003173616 A1 Div ex US 6545312; US
     6642572 B2 Div ex US 6545312; US 2004071024 A1 Div ex US 6545312, Div ex
     US 6642572
PRAI JP 2000-200579         20000703
IC   ICM  G11C007-00; H01L021-336; H01L021-8247; H01L027-115; H01L029-76;
          H01L029-788
     ICS  H01L021-3205; H01L021-4763; H01L021-8234; H01L027-088; H01L029-423;
          H01L029-792
AB   EP    1172856 A UPAB: 20020613
     NOVELTY - A protective insulating film (14) is deposited on side surfaces
     of a control gate electrode (13) formed on a substrate (11) with gate
     oxide film (12). A floating gate electrode (15) is formed opposite to a
     side surface of control gate electrode. A tunnel insulating film (16) is
     formed between floating gate electrode and substrate. Drain and source
     regions (11b,11a) are oppositively formed in substrate.
          DETAILED DESCRIPTION - An INDEPENDENT CLAIM is also included for
     non-volatile semiconductor memory fabrication method.
          USE - For fabricating non-volatile semiconductor memory e.g.
     split/stacked gate flash EEPROM (FEEPROM), used in electronic equipment.
          ADVANTAGE - Since the protective insulating film is deposited on side
     surfaces of control electrode the configuration of control electrode is
     not impaired during formation of floating gate electrode.
          DESCRIPTION OF DRAWING(S) - The figure shows a cross-sectional view
     of memory element in non-volatile semiconductor memory.
     Substrate 11
          Drain and source regions 11a,11b
          Gate oxide film 12
          Control gate electrode 13
          Protective insulating film 14
          Floating gate electrode 15
          Tunnel insulating film 16
     Dwg.1/58
FS   EPI
FA   AB; GI
MC   EPI: U11-C18B5; U12-E; U13-C04B2; U14-A03B7

L1     ANSWER 2 OF 9  INPADOC  COPYRIGHT 2004 EPO on STN

LEVEL 1
AN     232294967 INPADOC  ED 20040503  EW 200418  UP 20040503  UW 200418
TI     Nonvolatile semiconductor memory device and method for fabricating the
       same.
IN     KUSUMI MASATAKA; NORO FUMIHIKO; FUJIMOTO HIROMASA; KAMADA AKIHIRO;
       ODANAKA SHINJI; OGURA SEIKI
INS    KUSUMI MASATAKA; NORO FUMIHIKO; FUJIMOTO HIROMASA; KAMADA AKIHIRO;
       ODANAKA SHINJI; OGURA SEIKI
INA    JP; JP; JP; JP; JP; US
PA     MATSUSHITA ELECTRIC INDUSTRIAL CO., LTD.
PAS    MATSUSHITA ELECTRIC IND CO LTD
PAA    JP
DT     Patent
PIT    USAA PATENT APPLICATION PUBLICATION (PRE-GRANT)
PI     US 2004071024        AA 20040415
AI     US 2003-679431       A  20031007
PRAI   US 2003-679431       A  20031007
         JP 2000-200579       A  20000703
       US 2003-382520       A3 20030307
       US 2001-897417       A3 20010703
ICM    (7) G11C007-00
EPC    H01L29/423D2B2; H01L29/788B6B
NCL    3652

L1     ANSWER 3 OF 9  INPADOC  COPYRIGHT 2004 EPO on STN

LEVEL 1
AN     217337559 INPADOC  ED 20031014  EW 200341  UP 20031017  UW 200342
TI     Nonvolatile semiconductor memory device and method for fabricating the
       same.
IN     KUSUMI MASATAKA; NORO FUMIHIKO; FUJIMOTO HIROMASA; KAMADA AKIHIRO;
       ODANAKA SHINJI; OGURA SEIKI
INS    KUSUMI MASATAKA; NORO FUMIHIKO; FUJIMOTO HIROMASA; KAMADA AKIHIRO;
       ODANAKA SHINJI; OGURA SEIKI
INA    JP; JP; JP; JP; JP; US
PA     MATSUSHITA ELECTRIC INDUSTRIAL CO., LTD.
PAS    MATSUSHITA ELECTRIC IND CO LTD
PAA    JP
DT     Patent
PIT    USAA PATENT APPLICATION PUBLICATION (PRE-GRANT)
PI     US 2003173616        AA 20030918
AI     US 2003-382508       A  20030307
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PRAI   US 2003-382508       A  20030307
         JP 2000-200579       A  20000703
       US 2001-897417       A3 20010703
OSDW   2002-331812
ICM    (7) H01L029-788
EPC    H01L29/423D2B2; H01L29/788B6B
NCL    257316

L1     ANSWER 4 OF 9  INPADOC  COPYRIGHT 2004 EPO on STN

LEVEL 2
AN     212175639 INPADOC  ED 20031121  EW 200347  UP 20031205  UW 200349
TI     Nonvolatile semiconductor memory device and method for fabricating the
       same.
IN     KUSUMI MASATAKA; NORO FUMIHIKO; FUJIMOTO HIROMASA; KAMADA AKIHIRO;
       ODANAKA SHINJI; OGURA SEIKI
INS    KUSUMI MASATAKA; NORO FUMIHIKO; FUJIMOTO HIROMASA; KAMADA AKIHIRO;
       ODANAKA SHINJI; OGURA SEIKI
INA    JP; JP; JP; JP; JP; US
PA     MATSUSHITA ELECTRIC INDUSTRIAL CO., LTD.
PAS    MATSUSHITA ELECTRIC IND CO LTD
PAA    JP
DT     Patent
PIT    USBB PATENT (PREVIOUS PRE-GRANT PUBLICATION)
PI     US 6642572           BB 20031104
AI     US 2003-382520       A  20030307
PRAI   US 2003-382520       A  20030307
         JP 2000-200579       A  20000703
       US 2001-897417       A3 20010703
OSDW   2002-331812
ICM    (7) H01L029-788
EPC    H01L29/423D2B2; H01L29/788B6B
NCL    257315; X257316

L1     ANSWER 5 OF 9  INPADOC  COPYRIGHT 2004 EPO on STN

LEVEL 1
AN     211322662 INPADOC  ED 20030806  EW 200331  UP 20030806  UW 200331
TI     NONVOLATILE SEMICONDUCTOR MEMORY DEVICE AND METHOD FOR FABRICATING THE
       SAME.
IN     KUSUMI, MASATAKA; NORO, FUMIHIKO; FUJIMOTO, HIROMASA; KAMADA, AKIHIRO;
       ODANAKA, SHINJI
INS    KUSUMI MASATAKA; NORO FUMIHIKO; FUJIMOTO HIROMASA; KAMADA AKIHIRO;
       ODANAKA SHINJI
INA    JP; JP; JP; JP; JP
PA     MATSUSHITA ELECTRIC INDUSTRIAL CO., LTD.; HALO LSI DESIGN AND DEVICE
       TECHNOLOGIES INC.
PAS    MATSUSHITA ELECTRIC IND CO LTD; HALO LSI DESIGN AND DEVICE TEC
PAA    JP; US
TL     English
DT     Patent
PIT    TWB  PATENT
PI     TW 501284            B  20020901
AI     TW 2001-116264       A  20010703
PRAI   JP 2000-200579       A  20000703
ICM    (7) H01L029-788
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L1     ANSWER 6 OF 9  INPADOC  COPYRIGHT 2004 EPO on STN

LEVEL 1
AN     174007221 INPADOC  ED 20020507  EW 200218  UP 20020822  UW 200233
TI     NONVOLATILE SEMICONDUCTOR MEMORY DEVICE AND PRODUCTION METHOD THEREFOR.
IN     KUSUMI MASATAKA; NORO FUMIHIKO; FUJIMOTO HIROMASA; KAMATA AKIHIRO;
       ODANAKA SHINJI; OGURA SEIKI
INS    KUSUMI MASATAKA; NORO FUMIHIKO; FUJIMOTO HIROMASA; KAMATA AKIHIRO;
       ODANAKA SHINJI; OGURA SEIKI
PA     MATSUSHITA ELECTRIC IND CO LTD; HALO LSI DESIGN & DEVICE TECHNOL INC
PAS    MATSUSHITA ELECTRIC IND CO LTD; HALO LSI DESIGN & DEVICE TECHN
TL     English
DT     Patent
PIT    JPA2 DOCUMENT LAID OPEN TO PUBLIC INSPECTION
PI     JP 2002083886        A2 20020322
AI     JP 2001-150649       A  20010521
PRAI   JP 2001-150649       A  20010521
         JP 2000-200579       A  20000703
ICM    (7) H01L021-8247
ICS    (7) H01L021-8234; (7) H01L027-088; (7) H01L027-115;
       (7) H01L029-788; (7) H01L029-792

L1     ANSWER 7 OF 9  INPADOC  COPYRIGHT 2004 EPO on STN

LEVEL 2
AN     173146999 INPADOC  ED 20030505  EW 200317  UP 20030505  UW 200317
TI     NONVOLATILE SEMICONDUCTOR MEMORY DEVICE AND METHOD FOR FABRICATING THE
       SAME.
IN     KUSUMI MASATAKA; NORO FUMIHIKO; FUJIMOTO HIROMASA; KAMADA AKIHIRO;
       ODANAKA SHINJI; OGURA SEIKI
INS    KUSUMI MASATAKA; NORO FUMIHIKO; FUJIMOTO HIROMASA; KAMADA AKIHIRO;
       ODANAKA SHINJI; OGURA SEIKI
INA    JP; JP; JP; JP; JP; US
PA     MATSUSHITA ELECTRIC INDUSTRIAL CO., LTD.; HALO LSI DESIGN AND DEVICE
       TECHNOLOGIES INC.
PAS    MATSUSHITA ELECTRIC IND CO LTD; HALO LSI DESIGN AND DEVICE TEC
PAA    JP; US
DT     Patent
PIT    USBB PATENT (PREVIOUS PRE-GRANT PUBLICATION)
PI     US 6545312           BB 20030408
AI     US 2001-897417       A  20010703
PRAI   JP 2000-200579       A  20000703
ICM    (7) H01L029-788
ICS    (7) H01L029-792
EPC    H01L29/423D2B2; H01L29/788B6B
NCL    257315; X257324

L1     ANSWER 8 OF 9  INPADOC  COPYRIGHT 2004 EPO on STN

LEVEL 1
AN     166113123 INPADOC  ED 20020121  EW 200203  UP 20021007  UW 200240
TI     NONVOLATILE SEMICONDUCTOR MEMORY DEVICE AND METHOD FOR FABRICATING THE
       SAME.
IN     KUSUMI, MASATAKA; NORO, FUMIHIKO; FUJIMOTO, HIROMASA; KAMADA, AKIHIRO;
       ODANAKA, SHINJI; OGURA, SEIKI
INS    KUSUMI MASATAKA; NORO FUMIHIKO; FUJIMOTO HIROMASA; KAMADA AKIHIRO;
       ODANAKA SHINJI; OGURA SEIKI
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INA   JP; JP; JP; JP; JP; US
PA    MATSUSHITA ELECTRIC INDUSTRIAL CO., LTD.; HALO LSI DESIGN AND DEVICE
      TECHNOLOGIES INC.
PAS   MATSUSHITA ELECTRIC IND CO LTD; HALO LSI DESIGN AND DEVICE TEC
PAA   JP; US
TL    English; French; German
LA    English
DT    Patent
PIT   EPA1 PUBL. OF APPLICATION WITH SEARCH REPORT
PI    EP 1172856          A1 20020116
DS    R:  AT BE CH CY DE DK ES FI FR GB GR IE IT LI LU MC NL PT SE TR
AI    EP 2001-116049      A  20010702
PRAI  JP 2000-200579      A  20000703
OSCA  136:094607
OSDW  2002-331812
ICM   (7) H01L027-115
ICS   (7) H01L021-8247; (7) H01L029-788; (7) H01L029-423;
      (7) H01L021-336
EPC   H01L29/423D2B2; H01L29/788B6B

L1   ANSWER 9 OF 9  JAPIO  (C) 2004 JPO  on STN
AN   2002-083886    JAPIO
TI   NONVOLATILE SEMICONDUCTOR MEMORY DEVICE AND PRODUCTION METHOD THEREFOR
IN   KUSUMI MASATAKA; NORO FUMIHIKO; FUJIMOTO HIROMASA; KAMATA AKIHIRO; ODANAKA
     SHINJI; OGURA SEIKI
PA   MATSUSHITA ELECTRIC IND CO LTD
     HALO LSI DESIGN & DEVICE TECHNOL INC
PI   JP 2002083886 A  20020322 Heisei
AI   JP 2001-150649 (JP2001150649 Heisei) 20010521
PRAI JP 2000-20057920000703
SO   PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined Applications, Vol. 2002
IC   ICM  H01L021-8247
     ICS  H01L021-8234; H01L027-088; H01L027-115; H01L029-788; H01L029-792
AB   PROBLEM TO BE SOLVED: To surely form the memory cell of a split gate type
     nonvolatile semiconductor memory device and to prevent the operation
     characteristics of an MOS transistor from being affected by the memory
     cell when forming the memory cell on the same semiconductor wafer as the
     MOS transistor.
     SOLUTION: A control gate electrode 13 composed of a polycrystal silicon is
     formed on a semiconductor wafer 11 composed of a silicon through a gate
     oxide film 12. On both the side faces of the control gate electrode 13,
     the laminate of silicon oxide film and silicon nitride film is deposited
     for the film thickness of about 7 nm, and a protecting and insulating film
     14 is formed for protecting the control gate electrode 13 when forming a
     floating gate electrode 15. On one side face of the control gate electrode
     13, the floating gate electrode 15 of capacitive coupling with the control
     gate electrode 13 is formed while facing the control gate electrode
     through the protecting and insulating film 14.
     COPYRIGHT: (C)2002,JPO
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